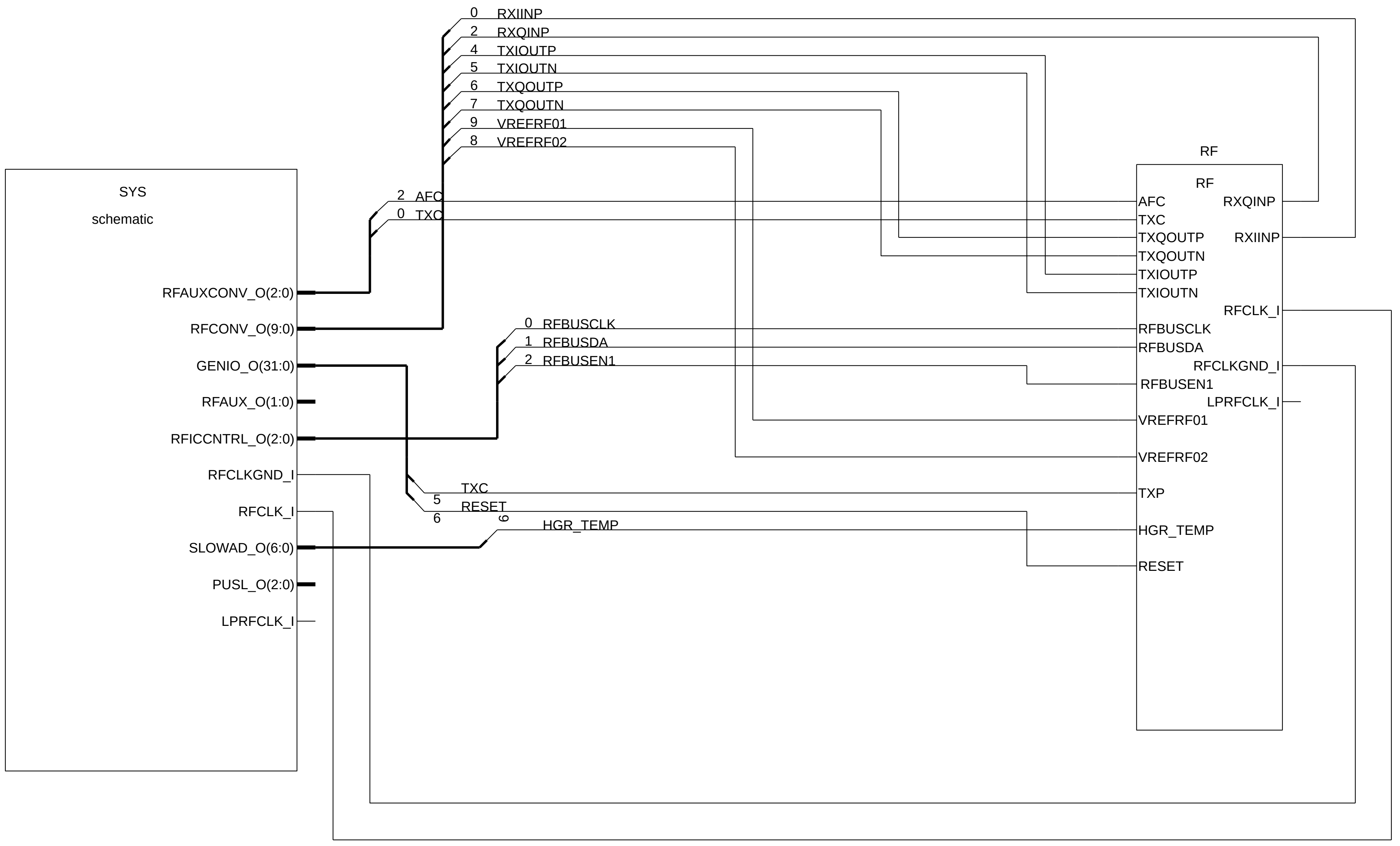
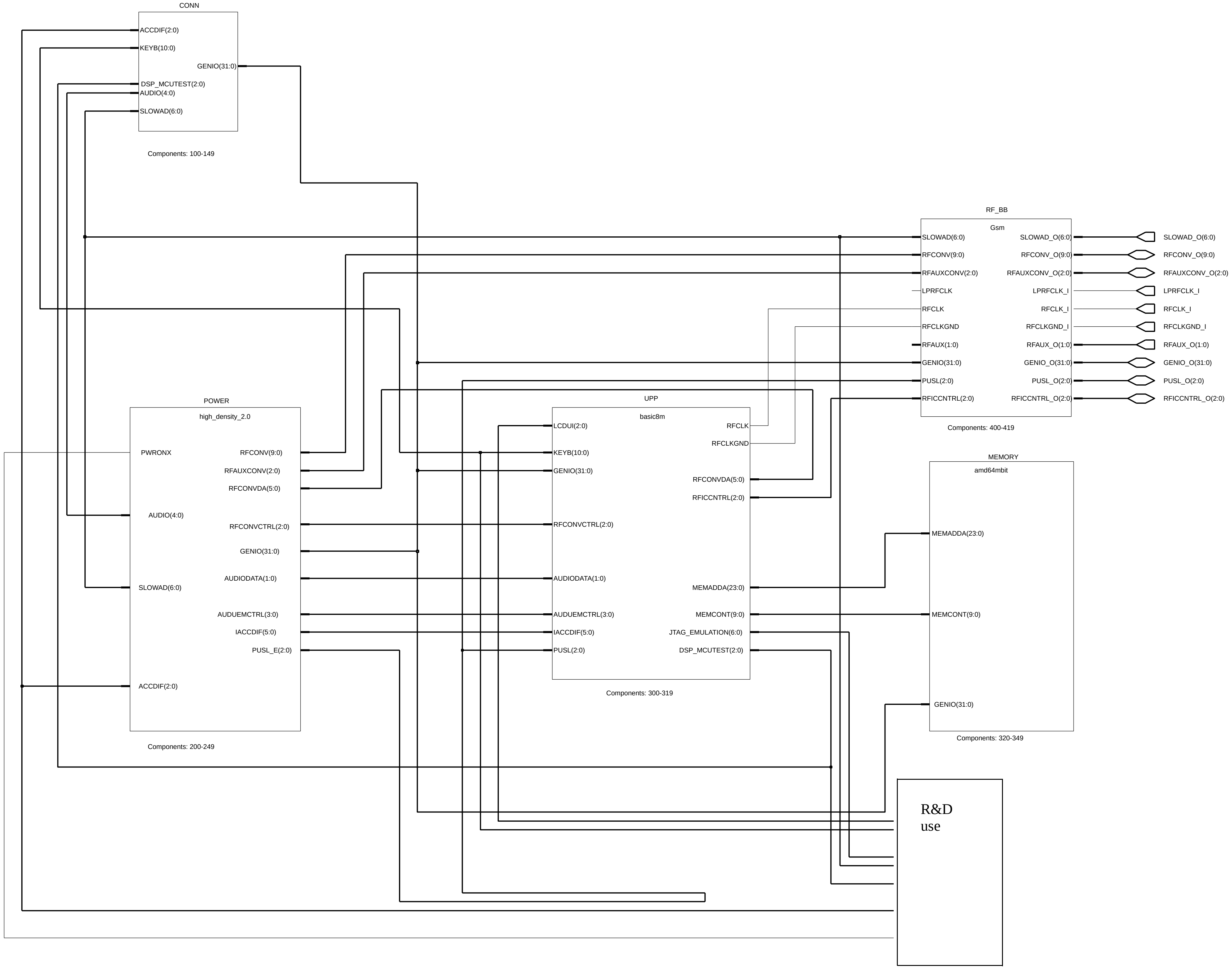
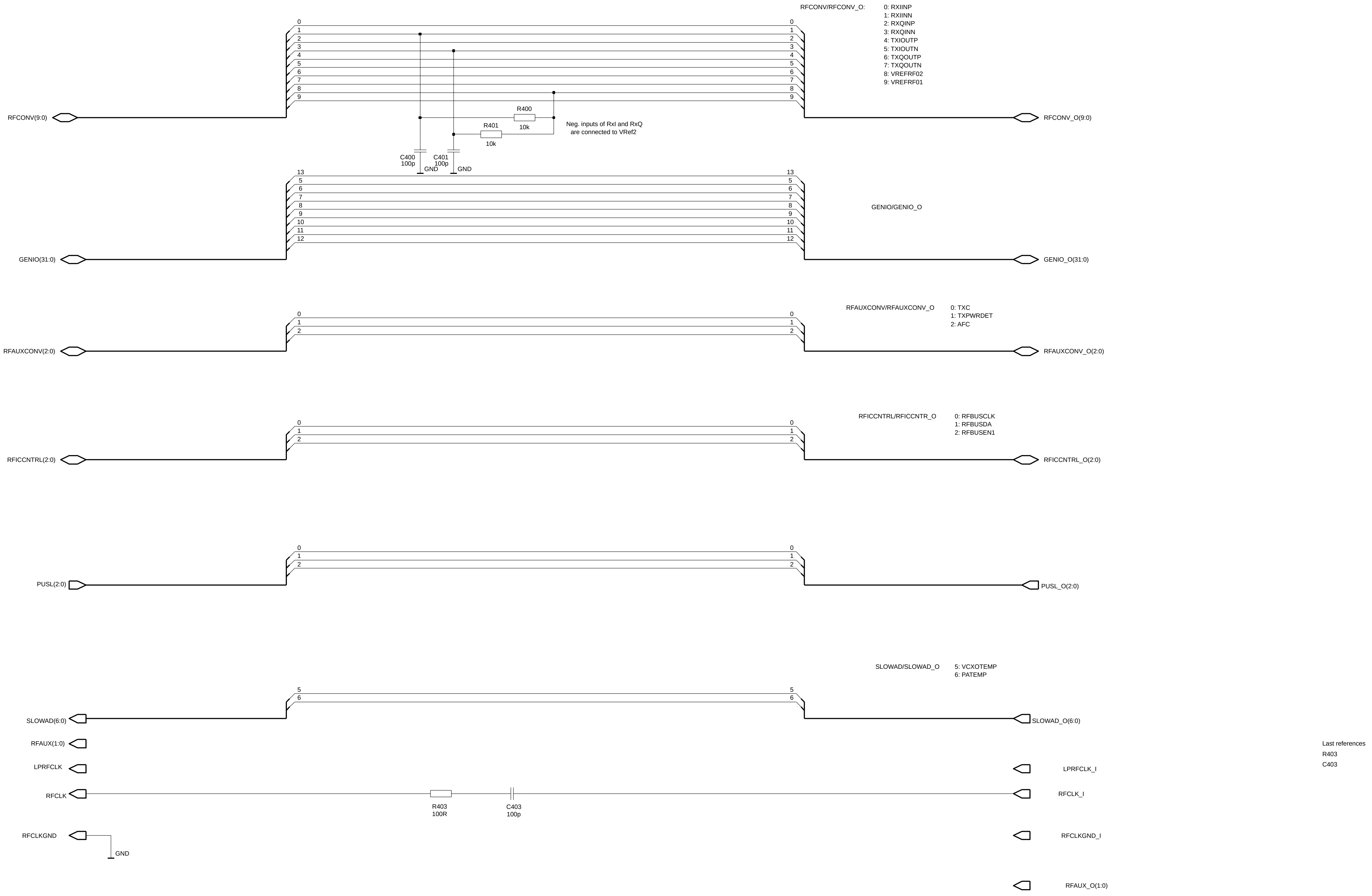
Block diagram v.RB5.0 ed.76


SYS
schematic
RFAUXCONV_O(2:0)
RFCONV_O(9:0)
GENIO_O(31:0)
RFAUX_O(1:0)
RFICCNTRL_O(2:0)
RFCLKGND_I
RFCLK_I
SLOWAD_O(6:0)
PUSL_O(2:0)
LPRFCLK_I
0 RXIINP
2 RXQINP
4 TXIOUTP
5 TXIOUTN
6 TXQOUTP
7 TXQOUTN
9 VREFRF01
8 VREFRF02
2 AFC
0 TXC
0 RFBUSCLK
1 RFBUSDA
2 RFBUSEN1
TXC
5 RESET
6
6 HGR_TEMP
RF
RF
AFC
TXC
TXQOUTP
TXQOUTN
TXIOUTP
TXIOUTN
RFBUSCLK
RFBUSDA
RFBUSEN1
VREFRF01
VREFRF02
TXP
HGR_TEMP
RESET
RXQINP
RXIINP
RFCLK_I
RFCLKGND_I
LPRFCLK_I

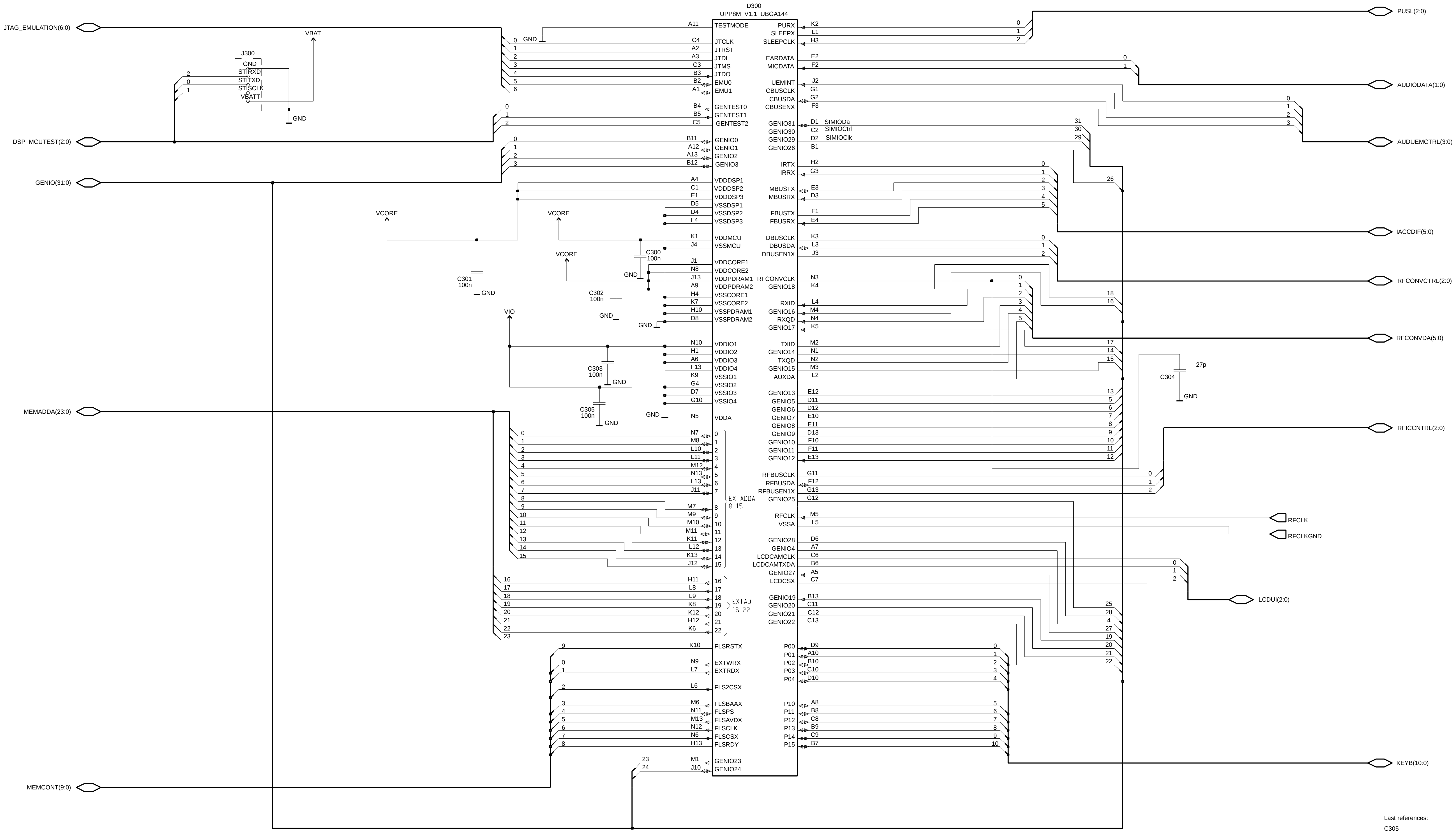
Block Diagram System v.RB5.0 ed.128


CONN
ACCDIF(2:0)
KEYB(10:0)
GENIO(31:0)
DSP_MCUTEST(2:0)
AUDIO(4:0)
SLOWAD(6:0)
Components: 100-149
RF_BB
Gsm
SLOWAD(6:0)
RFCONV(9:0)
RFAUXCONV(2:0)
LPRFCLK
RFCLK
RFCLKGND
RFAUX(1:0)
GENIO(31:0)
PUSL(2:0)
RFICCNTRL(2:0)
SLOWAD_O(6:0)
RFCONV_O(9:0)
RFAUXCONV_O(2:0)
LPRFCLK_I
RFCLK_I
RFCLKGND_I
RFAUX_O(1:0)
GENIO_O(31:0)
PUSL_O(2:0)
RFICCNTRL_O(2:0)
Components: 400-419
POWER
high_density_2.0
PWRONX
RFCONV(9:0)
RFAUXCONV(2:0)
RFCONVDA(5:0)
AUDIO(4:0)
RFCONVCTRL(2:0)
GENIO(31:0)
AUDIODATA(1:0)
SLOWAD(6:0)
AUDUEMCTRL(3:0)
IACCDIF(5:0)
PUSL_E(2:0)
ACCDIF(2:0)
Components: 200-249
UPP
basic8m
LCDUI(2:0)
KEYB(10:0)
GENIO(31:0)
RFCLK
RFCLKGND
RFCONVDA(5:0)
RFICCNTRL(2:0)
RFCONVCTRL(2:0)
AUDIODATA(1:0)
MEMADDA(23:0)
AUDUEMCTRL(3:0)
MEMCONT(9:0)
IACCDIF(5:0)
JTAG_EMULATION(6:0)
PUSL(2:0)
DSP_MCUTEST(2:0)
Components: 300-319
MEMORY
amd64mbit
MEMADDA(23:0)
MEMCONT(9:0)
GENIO(31:0)
Components: 320-349
R&D
use

Schematic diagram RF-BB v.RB5.0 ed.20

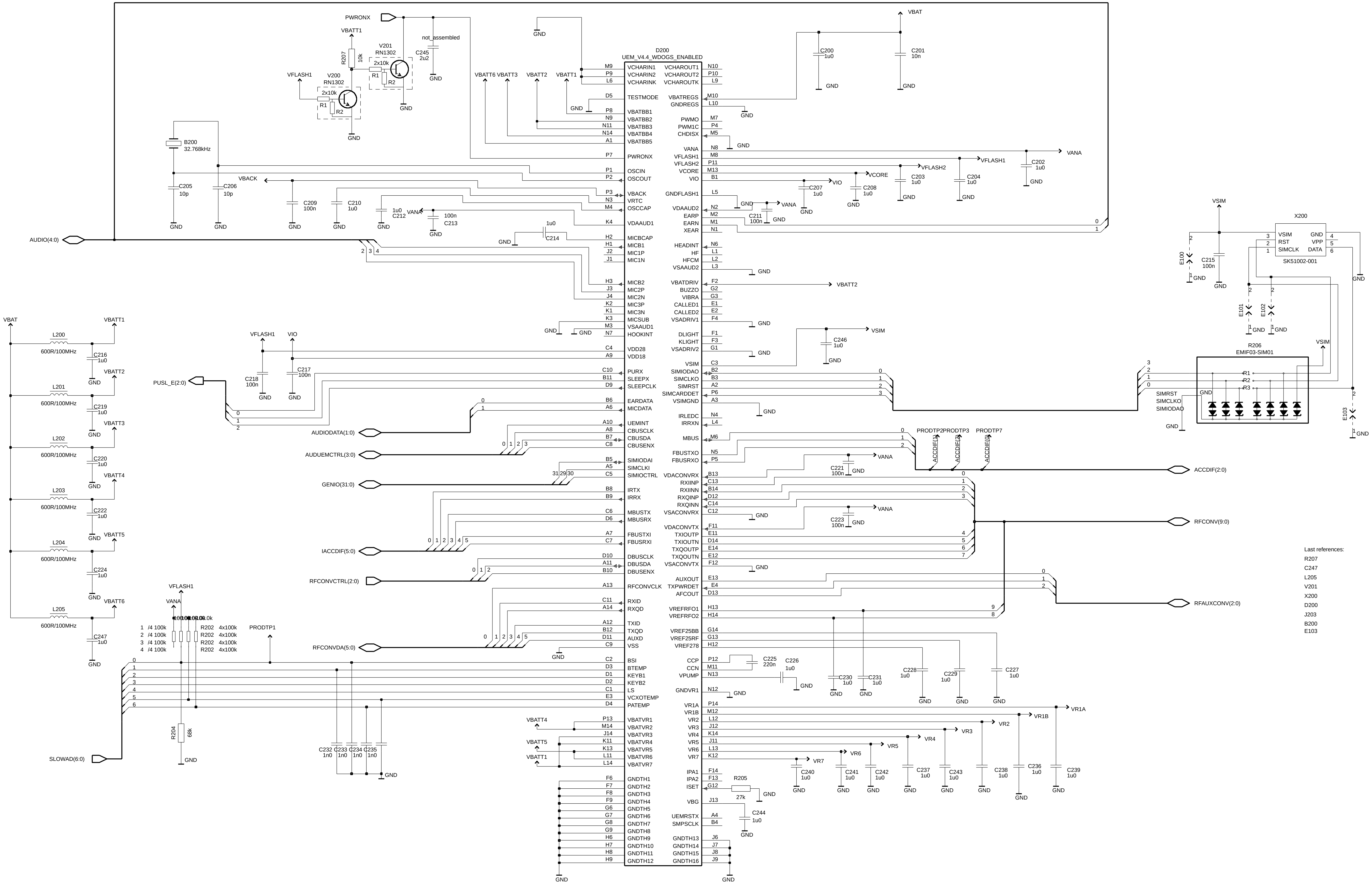

RFCONV/RFCONV_O:
0: RXIINP
1: RXIINN
2: RXQINP
3: RXQINN
4: TXIOUTP
5: TXIOUTN
6: TXQOUTP
7: TXQOUTN
8: VREFRF02
9: VREFRF01
RFCONV(9:0)
RFCONV_O(9:0)
R400
10k
R401
10k
Neg. inputs of RxI and RxQ
are connected to VRef2
C400
100p
C401
100p
GND
GND
GENIO/GENIO_O
GENIO(31:0)
GENIO_O(31:0)
RFAUXCONV/RFAUXCONV_O
0: TXC
1: TXPWRDET
2: AFC
RFAUXCONV(2:0)
RFAUXCONV_O(2:0)
RFICCNTRL/RFICCNTR_O
0: RFBUSCLK
1: RFBUSDA
2: RFBUSEN1
RFICCNTRL(2:0)
RFICCNTRL_O(2:0)
PUSL(2:0)
PUSL_O(2:0)
SLOWAD/SLOWAD_O
5: VCXOTEMP
6: PATEMP
SLOWAD(6:0)
SLOWAD_O(6:0)
RFAUX(1:0)
LPRFCLK
LPRFCLK_I
RFCLK
RFCLK_I
R403
100R
C403
100p
RFCLKGND
GND
RFCLKGND_I
RFAUX_O(1:0)
Last references
R403
C403

Schematic Diagram UPP v.RB5.0 ed.26

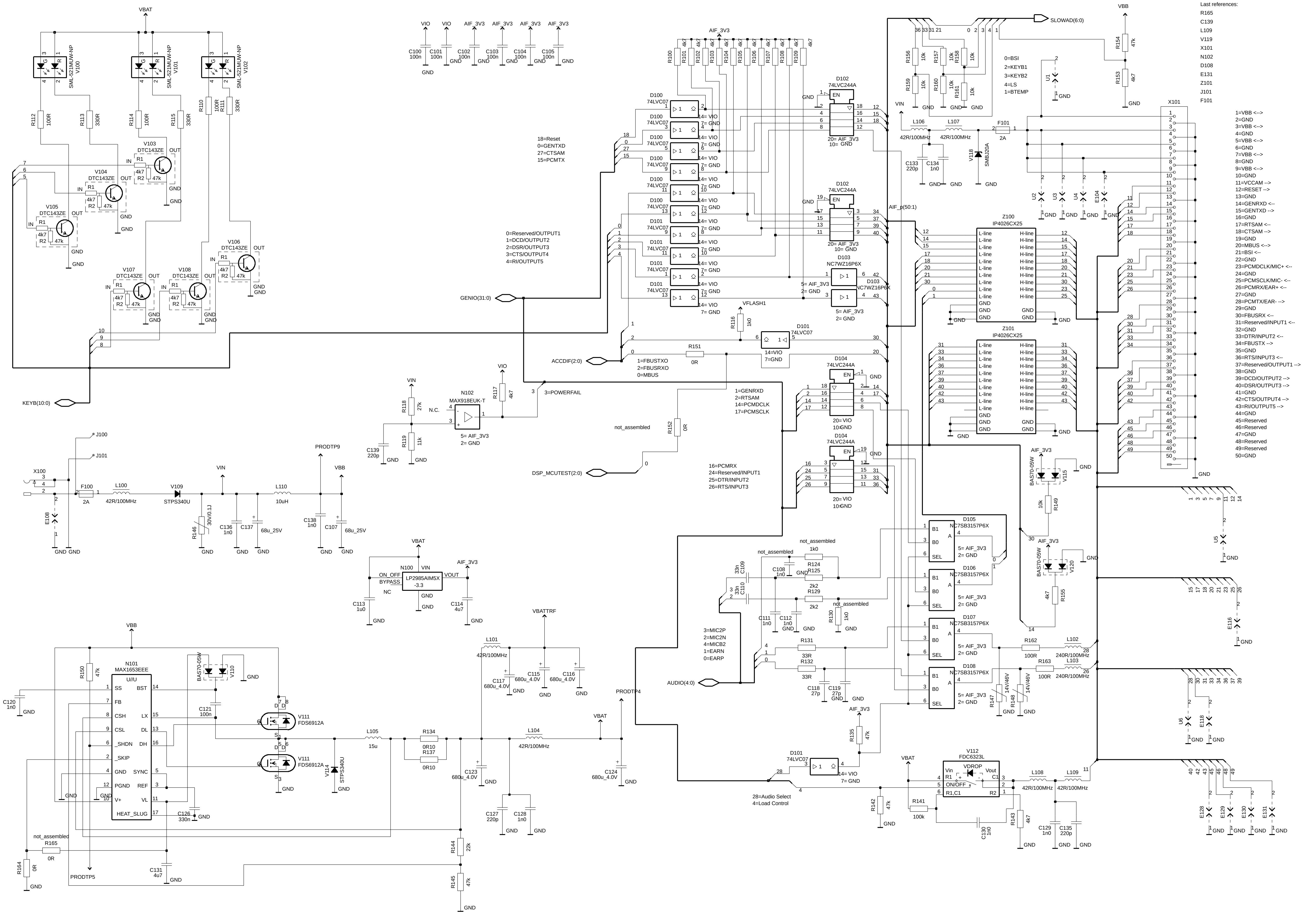

D300
UPP8M_V1.1_UBGA144
JTAG_EMULATION(6:0)
DSP_MCUTEST(2:0)
GENIO(31:0)
MEMADDA(23:0)
MEMCONT(9:0)
J300
GND
STIRXD
STITXD
STISCLK
VBATT
VBAT
VCORE
VIO
C300 100n
C301 100n
C302 100n
C303 100n
C305 100n
C304 27p
TESTMODE
JTCLK
JTRST
JTDI
JTMS
JTDO
EMU0
EMU1
GENTEST0
GENTEST1
GENTEST2
GENIO0
GENIO1
GENIO2
GENIO3
VDDDSP1
VDDDSP2
VDDDSP3
VSSDSP1
VSSDSP2
VSSDSP3
VDDMCU
VSSMCU
VDDCORE1
VDDCORE2
VDDPDRAM1
VDDPDRAM2
VSSCORE1
VSSCORE2
VSSPDRAM1
VSSPDRAM2
VDDIO1
VDDIO2
VDDIO3
VDDIO4
VSSIO1
VSSIO2
VSSIO3
VSSIO4
VDDA
EXTADDA 0:15
EXTAD 16:22
FLSRSTX
EXTWRX
EXTRDX
FLS2CSX
FLSBAAX
FLSPS
FLSAVDX
FLSCLK
FLSCSX
FLSRDY
GENIO23
GENIO24
PURX
SLEEPX
SLEEPCLK
EARDATA
MICDATA
UEMINT
CBUSCLK
CBUSDA
CBUSENX
GENIO31
GENIO30
GENIO29
GENIO26
SIMIODa
SIMIOCtrl
SIMIOClk
IRTX
IRRX
MBUSTX
MBUSRX
FBUSTX
FBUSRX
DBUSCLK
DBUSDA
DBUSEN1X
RFCONVCLK
GENIO18
RXID
GENIO16
RXQD
GENIO17
TXID
GENIO14
TXQD
GENIO15
AUXDA
GENIO13
GENIO5
GENIO6
GENIO7
GENIO8
GENIO9
GENIO10
GENIO11
GENIO12
RFBUSCLK
RFBUSDA
RFBUSEN1X
GENIO25
RFCLK
VSSA
GENIO28
GENIO4
LCDCAMCLK
LCDCAMTXDA
GENIO27
LCDCSX
GENIO19
GENIO20
GENIO21
GENIO22
P00
P01
P02
P03
P04
P10
P11
P12
P13
P14
P15
PUSL(2:0)
AUDIODATA(1:0)
AUDUEMCTRL(3:0)
IACCDIF(5:0)
RFCONVCTRL(2:0)
RFCONVDA(5:0)
RFICCNTRL(2:0)
RFCLK
RFCLKGND
LCDUI(2:0)
KEYB(10:0)
GND

Last references:
C305
X300
D300

Schematic Diagram UEM v. RB5.0 ed. 77

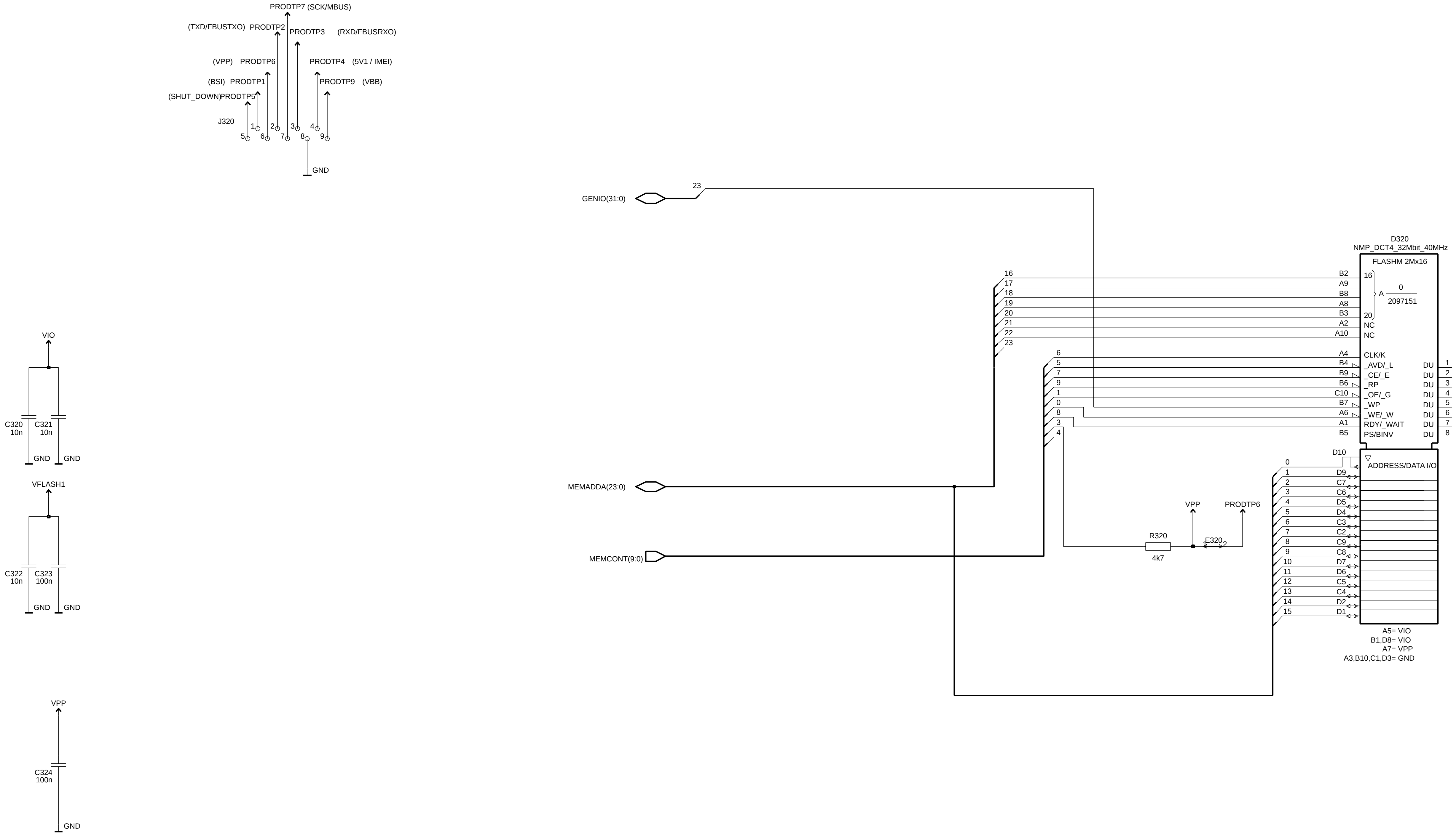

D200
UEM_V4.4_WDOGS_ENABLED
PWRONX
VBATT1
R207 10k
V201 RN1302
2x10k
R1
R2
C245 2u2
not_assembled
VFLASH1
V200 RN1302
GND
B200 32.768kHz
C205 10p
C206 10p
VBACK
C209 100n
C210 1u0
C212 1u0
VANA
C213 100n
C214 1u0
AUDIO(4:0)
VBAT
VBATT2
VBATT3
VBATT4
VBATT5
VBATT6
VBATT6 VBATT3 VBATT2 VBATT1
L200 600R/100MHz
L201 600R/100MHz
L202 600R/100MHz
L203 600R/100MHz
L204 600R/100MHz
L205 600R/100MHz
C216 1u0
C219 1u0
C220 1u0
C222 1u0
C224 1u0
C247 1u0
VIO
C218 100n
C217 100n
PUSL_E(2:0)
AUDIODATA(1:0)
AUDUEMCTRL(3:0)
GENIO(31:0)
IACCDIF(5:0)
RFCONVCTRL(2:0)
RFCONVDA(5:0)
SLOWAD(6:0)
PRODTP1
R202 4x100k
R204 68k
C232 1n0
C233 1n0
C234 1n0
C235 1n0
VCHARIN1 VCHARIN2 VCHARINK TESTMODE VBATBB1 VBATBB2 VBATBB3 VBATBB4 VBATBB5 PWRONX OSCIN OSCOUT VBACK VRTC OSCCAP VDAAUD1 MICBCAP MICB1 MIC1P MIC1N MICB2 MIC2P MIC2N MIC3P MIC3N MICSUB VSAAUD1 HOOKINT VDD28 VDD18 PURX SLEEPX SLEEPCLK EARDATA MICDATA UEMINT CBUSCLK CBUSDA CBUSENX SIMIODAI SIMCLKI SIMIOCTRL IRTX IRRX MBUSTX MBUSRX FBUSTXI FBUSRXI DBUSCLK DBUSDA DBUSENX RFCONVCLK RXID RXQD TXID TXQD AUXD VSS BSI BTEMP KEYB1 KEYB2 LS VCXOTEMP PATEMP VBATVR1 VBATVR2 VBATVR3 VBATVR4 VBATVR5 VBATVR6 VBATVR7 GNDTH1 GNDTH2 GNDTH3 GNDTH4 GNDTH5 GNDTH6 GNDTH7 GNDTH8 GNDTH9 GNDTH10 GNDTH11 GNDTH12
VCHAROUT1 VCHAROUT2 VCHAROUTK VBATREGS GNDREGS PWMO PWM1C CHDISX VANA VFLASH1 VFLASH2 VCORE VIO GNDFLASH1 VDAAUD2 EARP EARN XEAR HEADINT HF HFCM VSAAUD2 VBATDRIV BUZZO VIBRA CALLED1 CALLED2 VSADRIV1 DLIGHT KLIGHT VSADRIV2 VSIM SIMIODAO SIMCLKO SIMRST SIMCARDDET VSIMGND IRLEDC IRRXN MBUS FBUSTXO FBUSRXO VDACONVRX RXIINP RXIINN RXQINP RXQINN VSACONVRX VDACONVTX TXIOUTP TXIOUTN TXQOUTP TXQOUTN VSACONVTX AUXOUT TXPWRDET AFCOUT VREFRFO1 VREFRFO2 VREF25BB VREF25RF VREF278 CCP CCN VPUMP GNDVR1 VR1A VR1B VR2 VR3 VR4 VR5 VR6 VR7 IPA1 IPA2 ISET VBG UEMRSTX SMPSCLK GNDTH13 GNDTH14 GNDTH15 GNDTH16
C200 1u0
C201 10n
C202 1u0
C203 1u0
C204 1u0
C207 1u0
C208 1u0
C211 100n
C246 1u0
C221 100n
C223 100n
C225 220n
C226 1u0
C227 1u0
C228 1u0
C229 1u0
C230 1u0
C231 1u0
C236 1u0
C237 1u0
C238 1u0
C239 1u0
C240 1u0
C241 1u0
C242 1u0
C243 1u0
C244 1u0
R205 27k
VSIM
X200
SK51002-001
VSIM RST SIMCLK GND VPP DATA
C215 100n
E100
E101
E102
E103
R206 EMIF03-SIM01
SIMRST SIMCLKO SIMIODAO
PRODTP2 PRODTP3 PRODTP7
ACCDIF(1) ACCDIF(0) ACCDIF(0)
ACCDIF(2:0)
RFCONV(9:0)
RFAUXCONV(2:0)
Last references:
R207
C247
L205
V201
X200
D200
J203
B200
E103

Schematic diagram AIF, PWR, LED v. RB5.0 ed.132


VBAT
SML-521MUW-NP V100
SML-521MUW-NP V101
SML-521MUW-NP V102
R112 100R
R113 330R
R114 100R
R115 330R
R110 100R
R111 330R
V103 DTC143ZE
V104 DTC143ZE
V105 DTC143ZE
V106 DTC143ZE
V107 DTC143ZE
V108 DTC143ZE
IN
OUT
R1 4k7
R2 47k
GND
KEYB(10:0)
VIO
AIF_3V3
C100 100n
C101 100n
C102 100n
C103 100n
C104 100n
C105 100n
18=Reset
0=GENTXD
27=CTSAM
15=PCMTX
0=Reserved/OUTPUT1
1=DCD/OUTPUT2
2=DSR/OUTPUT3
3=CTS/OUTPUT4
4=RI/OUTPUT5
GENIO(31:0)
ACCDIF(2:0)
1=FBUSTXO
2=FBUSRXO
0=MBUS
R151 0R
R152 0R
not_assembled
DSP_MCUTEST(2:0)
3=POWERFAIL
N102 MAX918EUK-T
N.C.
R117 4k7
R118 27k
R119 11k
C139 220p
5= AIF_3V3
2= GND
PRODTP9
J100
J101
X100
E108
F100 2A
L100 42R/100MHz
V109 STPS340U
VIN
VBB
R146 30V/0.1J
C136 1n0
C137
68u_25V
L110 10uH
C138 1n0
C107 68u_25V
N100 LP2985AIM5X -3.3
ON_OFF
BYPASS
NC
VOUT
C113 1u0
C114 4u7
VBATTRF
L101 42R/100MHz
C117 680u_4.0V
C115 680u_4.0V
C116 680u_4.0V
N101 MAX1653EEE
SS
FB
CSH
CSL
_SHDN
_SKIP
GND
PGND
V+
BST
LX
DL
DH
SYNC
REF
VL
HEAT_SLUG
R150 47k
C120 1n0
BAS70-05W V110
C121 100n
V111 FDS6912A
V114 STPS340U
L105 15u
R134 0R10
R137 0R10
L104 42R/100MHz
C123 680u_4.0V
C124 680u_4.0V
C127 220p
C128 1n0
C126 330n
C131 4u7
R144 22k
R145 47k
R164 0R
R165 0R
PRODTP5
PRODTP4
AIF_3V3
R100 4k7
R101 4k7
R102 4k7
R103 4k7
R104 4k7
R105 4k7
R106 4k7
R107 4k7
R108 4k7
R109 4k7
D100 74LVC07
D101 74LVC07
14= VIO
7= GND
D102 74LVC244A
EN
20= AIF_3V3
10= GND
D103 NC7WZ16P6X
5= AIF_3V3
R116 1k0
VFLASH1
D101 74LVC07
14=VIO
7=GND
D104 74LVC244A
20= VIO
10 GND
1=GENRXD
2=RTSAM
14=PCMDCLK
17=PCMSCLK
16=PCMRX
24=Reserved/INPUT1
25=DTR/INPUT2
26=RTS/INPUT3
C109 33n
C110 33n
not_assembled
R124 1k0
R125 2k2
R129 2k2
R130 1k0
C108 1n0
C111 1n0
C112 1n0
3=MIC2P
2=MIC2N
4=MICB2
1=EARN
0=EARP
AUDIO(4:0)
R131 33R
R132 33R
C118 27p
C119 27p
R135 47k
28=Audio Select
4=Load Control
D105 NC7SB3157P6X
D106 NC7SB3157P6X
D107 NC7SB3157P6X
D108 NC7SB3157P6X
B1
B0
SEL
A
R162 100R
R163 100R
L102 240R/100MHz
L103 240R/100MHz
R147 14V/46V
R148 14V/46V
V112 FDC6323L
Vin
VDROP
Vout
R1
ON/OFF
R1,C1
R2
C1
R142 47k
R141 100k
R143 4k7
C130 1n0
L108 42R/100MHz
L109 42R/100MHz
C129 1n0
C135 220p
E128
E129
E130
E131
SLOWAD(6:0)
R156 10k
R157 10k
R158 10k
R159 10k
R160 10k
R161 10k
0=BSI
2=KEYB1
3=KEYB2
4=LS
1=BTEMP
U1
L106 42R/100MHz
L107 42R/100MHz
F101 2A
C133 220p
C134 1n0
V118 SMBJ20A
AIF_p(50:1)
U2
U3
U4
E104
Z100 IP4026CX25
Z101 IP4026CX25
L-line
H-line
BAS70-05W V115
BAS70-05W V120
R149 10k
R155 4k7
U5
E116
U6
E118
R154 47k
R153 4k7
X101
Last references:
R165
C139
L109
V119
X101
N102
D108
E131
Z101
J101
F101
1=VBB <-->
2=GND
3=VBB <-->
4=GND
5=VBB <-->
6=GND
7=VBB <-->
8=GND
9=VBB <-->
10=GND
11=VCCAM -->
12=RESET -->
13=GND
14=GENRXD <--
15=GENTXD -->
16=GND
17=RTSAM <--
18=CTSAM -->
19=GND
20=MBUS <-->
21=BSI <--
22=GND
23=PCMDCLK/MIC+ <--
24=GND
25=PCMSCLK/MIC- <--
26=PCMRX/EAR+ <--
27=GND
28=PCMTX/EAR- -->
29=GND
30=FBUSRX <--
31=Reserved/INPUT1 <--
32=GND
33=DTR/INPUT2 <--
34=FBUSTX -->
35=GND
36=RTS/INPUT3 <--
37=Reserved/OUTPUT1 -->
38=GND
39=DCD/OUTPUT2 -->
40=DSR/OUTPUT3 -->
41=GND
42=CTS/OUTPUT4 -->
43=RI/OUTPUT5 -->
44=GND
45=Reserved
46=Reserved
47=GND
48=Reserved
49=Reserved
50=GND

Schematic Diagram Memories v. RB5.0 ed.24

Last references:
R320
C324
D320
E320
J320


PRODTP7 (SCK/MBUS)
(TXD/FBUSTXO) PRODTP2
PRODTP3 (RXD/FBUSRXO)
(VPP) PRODTP6
PRODTP4 (5V1 / IMEI)
(BSI) PRODTP1
PRODTP9 (VBB)
(SHUT_DOWN) PRODTP5
J320
GND
GENIO(31:0)
23
MEMADDA(23:0)
MEMCONT(9:0)
D320
NMP_DCT4_32Mbit_40MHz
FLASHM 2Mx16
A
0
2097151
NC
CLK/K
_AVD/_L
_CE/_E
_RP
_OE/_G
_WP
_WE/_W
RDY/_WAIT
PS/BINV
DU
ADDRESS/DATA I/O
D10
VPP
PRODTP6
R320
4k7
E320
A5= VIO
B1,D8= VIO
A7= VPP
A3,B10,C1,D3= GND
VIO
C320 10n
C321 10n
VFLASH1
C322 10n
C323 100n
VPP
C324 100n
GND

Schematic Diagram RF, v. RB5.0 ed. 163

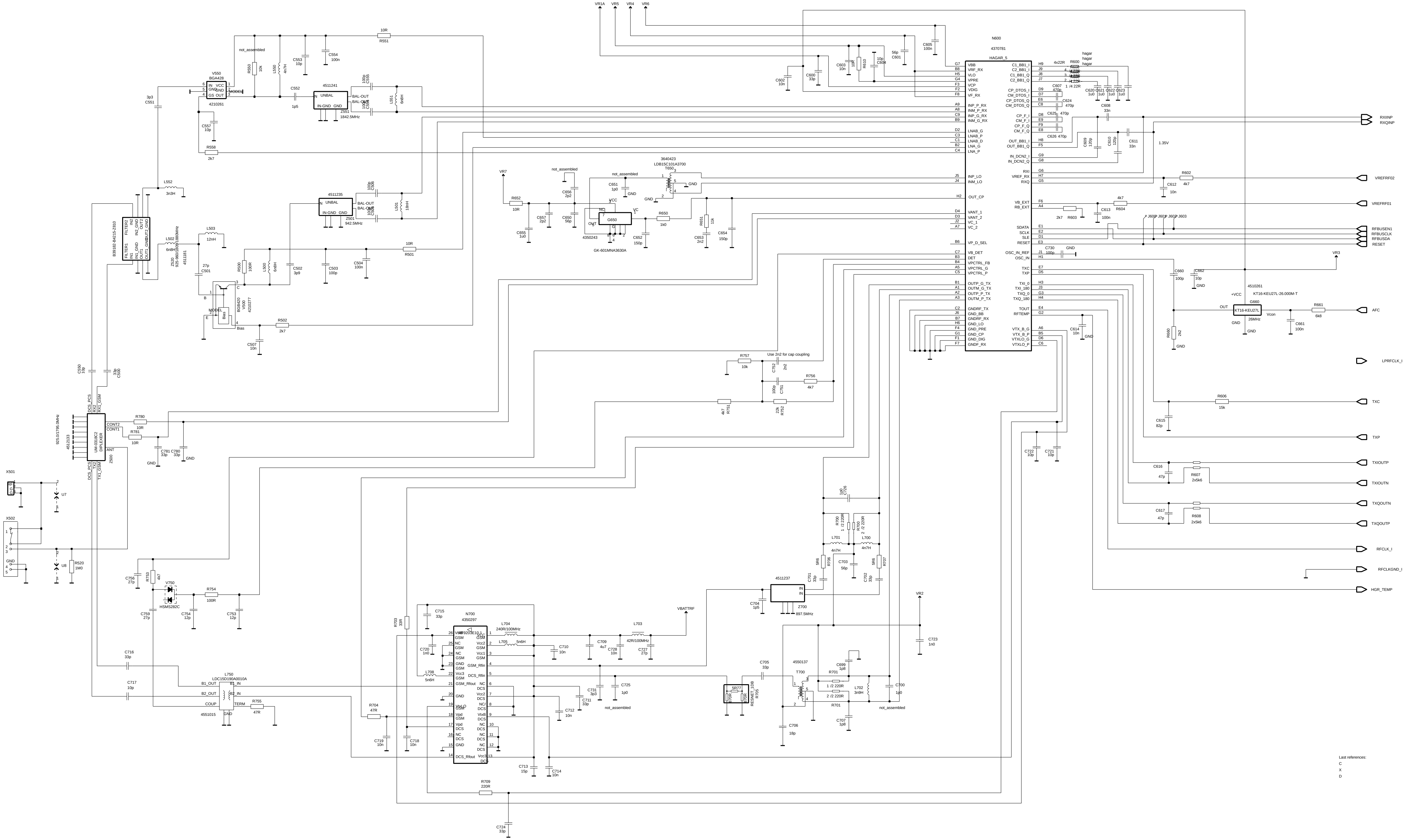
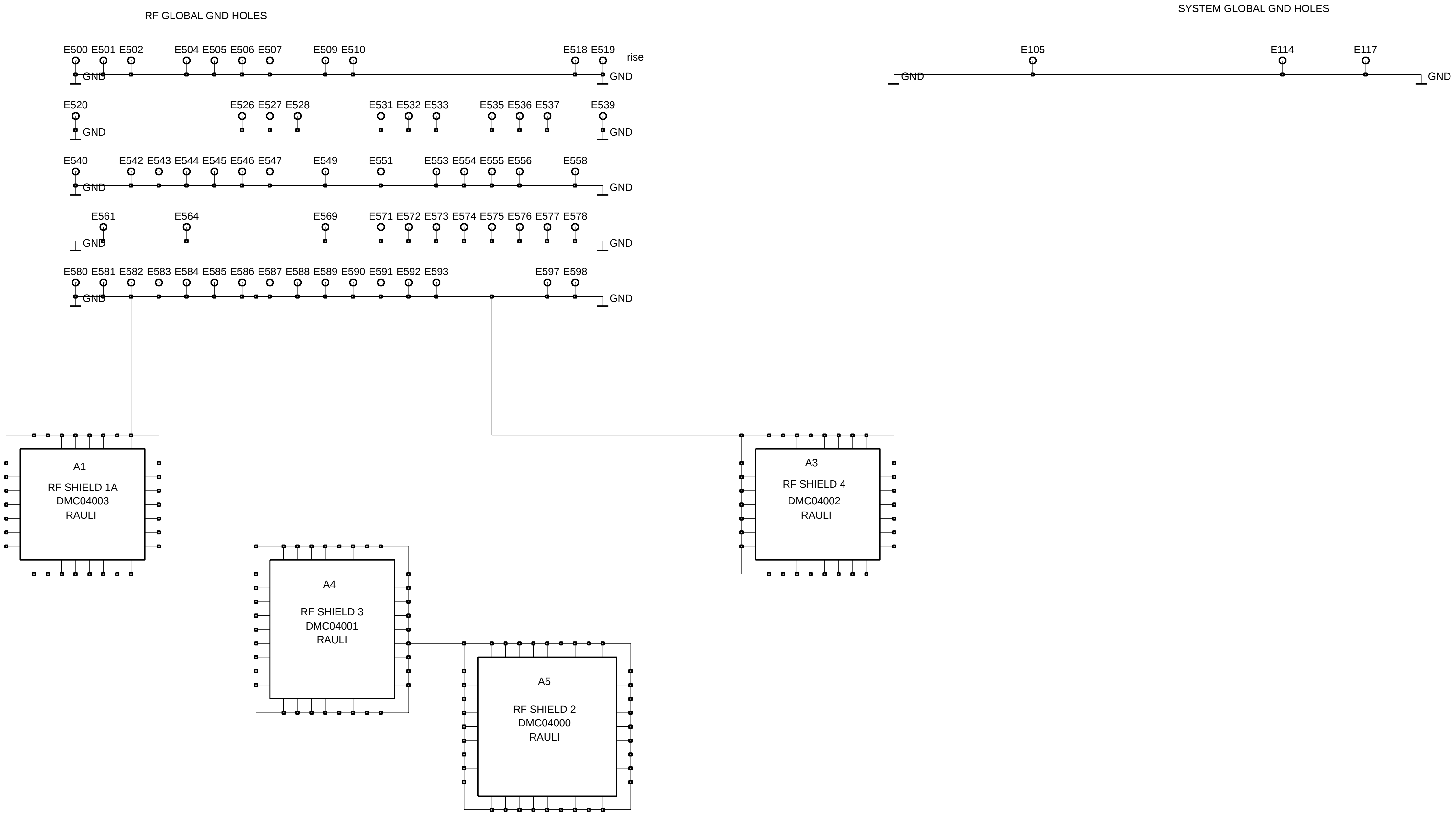
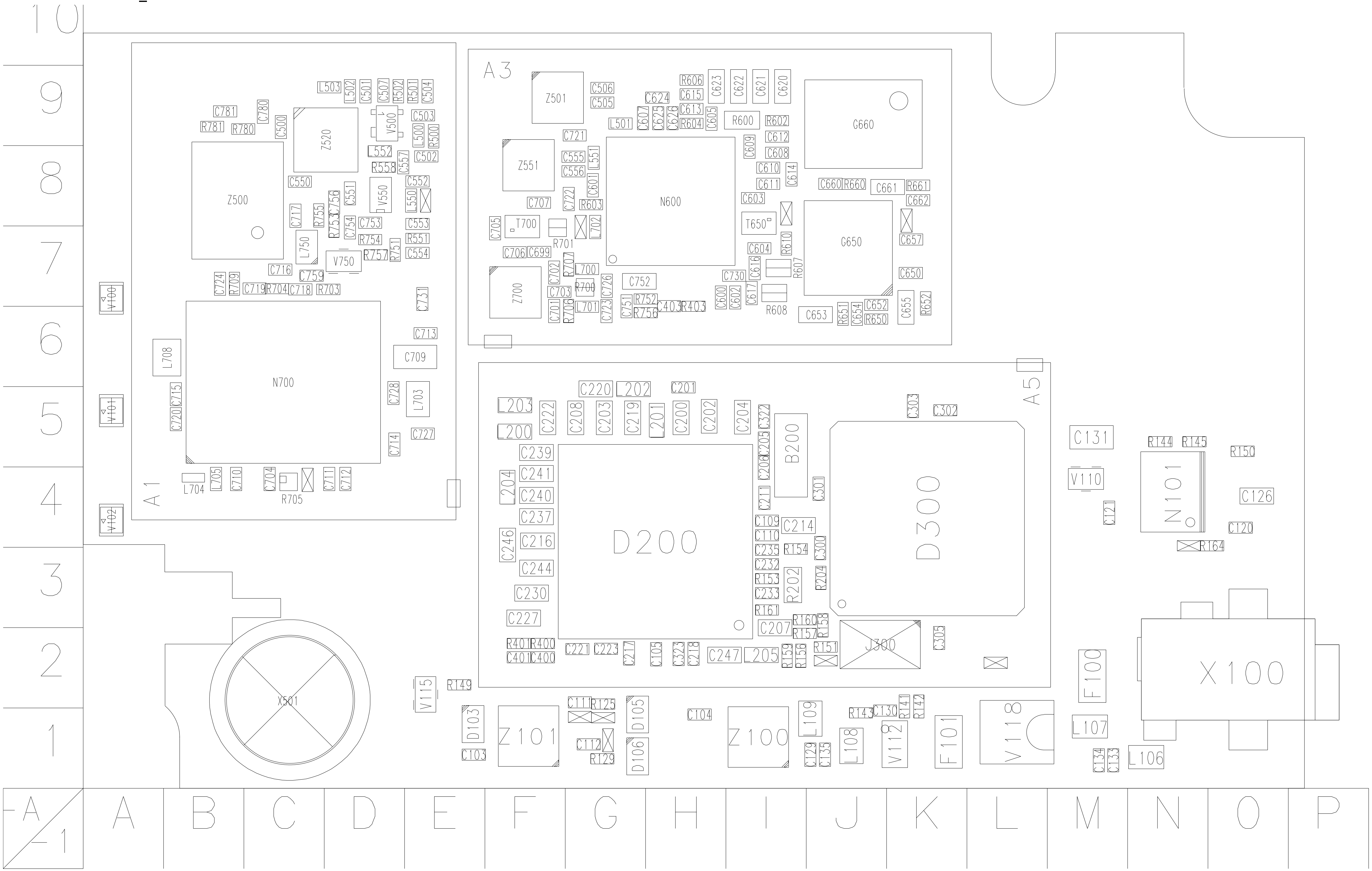

VR1A
VR5
VR4
VR6
N600
4370781
HAGAR_5
R551
10R
C554
100n
not_assembled
V550
BGA428
4210261
R550
10k
L550
4n7H
C553
10p
C552
1p5
4511241
Z551
1842.5MHz
L551
6n8H
C551
3p3
C557
10p
R558
2k7
L552
3n3H
Z552
4511235
Z501
942.5MHz
L501
18nH
L503
12nH
L502
6n8H
Z520
925-960/1805-1880MHz
4511181
R501
10R
C503
100p
C504
100n
C502
3p9
R500
100R
L500
6n8H
C501
27p
V500
BGR420
4210277
R502
2k7
C507
10n
C500
33p
C550
10p
R780
10R
R781
10R
C781
33p
C780
33p
Z600
DIPLEXER
4511210
925.0/1795.0MHz
X501
X502
U7
U8
R520
1M0
VR7
R652
10R
C655
1u0
C657
2p2
C656
2p2
C650
56p
G650
4350243
GK-601MNA3630A
C651
1p0
T650
3640423
LDB15C101A3700
R650
1k0
C652
150p
C653
2n2
R651
11k
C654
150p
R602
4k7
C612
10n
R604
4k7
R603
2k7
C613
100n
C730
100p
C660
100p
C662
10p
G660
KT16-KEU27L
4510261
KT16-KEU27L-26.000M-T
26MHz
R661
6k8
C661
100n
R660
2k2
C614
10n
C611
33n
C610
120p
C609
120p
C608
33n
1.35V
C626
470p
C625
470p
C624
470p
C607
470p
R606
15k
C615
82p
C616
47p
R607
2x5k6
C617
47p
R608
2x5k6
C722
10p
C721
10p
R757
10k
C752
2n2
Use 2n2 for cap coupling
R756
4k7
C751
100p
R751
4k7
R752
22k
C726
1p0
R700
1 /2 220R
L701
4n7H
L700
4n7H
R706
5R6
R707
5R6
C703
56p
C701
33p
C702
33p
4511237
Z700
897.5MHz
C704
1p5
VR2
C723
1n0
VBATTRF
L703
42R/100MHz
C709
4u7
C728
10n
C727
27p
N700
4350297
L704
240R/100MHz
L705
5n6H
C710
10n
C715
33p
C720
1n0
L708
5n6H
R703
33R
C725
1p0
C731
3p3
C711
33p
C712
10n
not_assembled
C705
33p
4550137
T700
R701
1 /2 220R
2 /2 220R
C699
1p8
L702
3n9H
C700
1p0
C707
1p8
C706
18p
R705
C719
10n
C718
10n
R704
47R
C713
15p
C714
10n
R709
220R
C724
33p
L750
LDC15D190A0010A
4551015
R755
47R
C716
33p
C717
10p
R754
100R
C753
12p
C754
12p
V750
HSMS282C
R753
4k7
C756
27p
C759
27p
RXINP
RXQINP
VREFRF02
VREFRF01
RFBUSEN1
RFBUSCLK
RFBUSDA
RESET
AFC
LPRFCLK_I
TXC
TXP
TXIOUTP
TXIOUTN
TXQOUTN
TXQOUTP
RFCLK_I
RFCLKGND_I
HGR_TEMP
Last references:
C
X
D

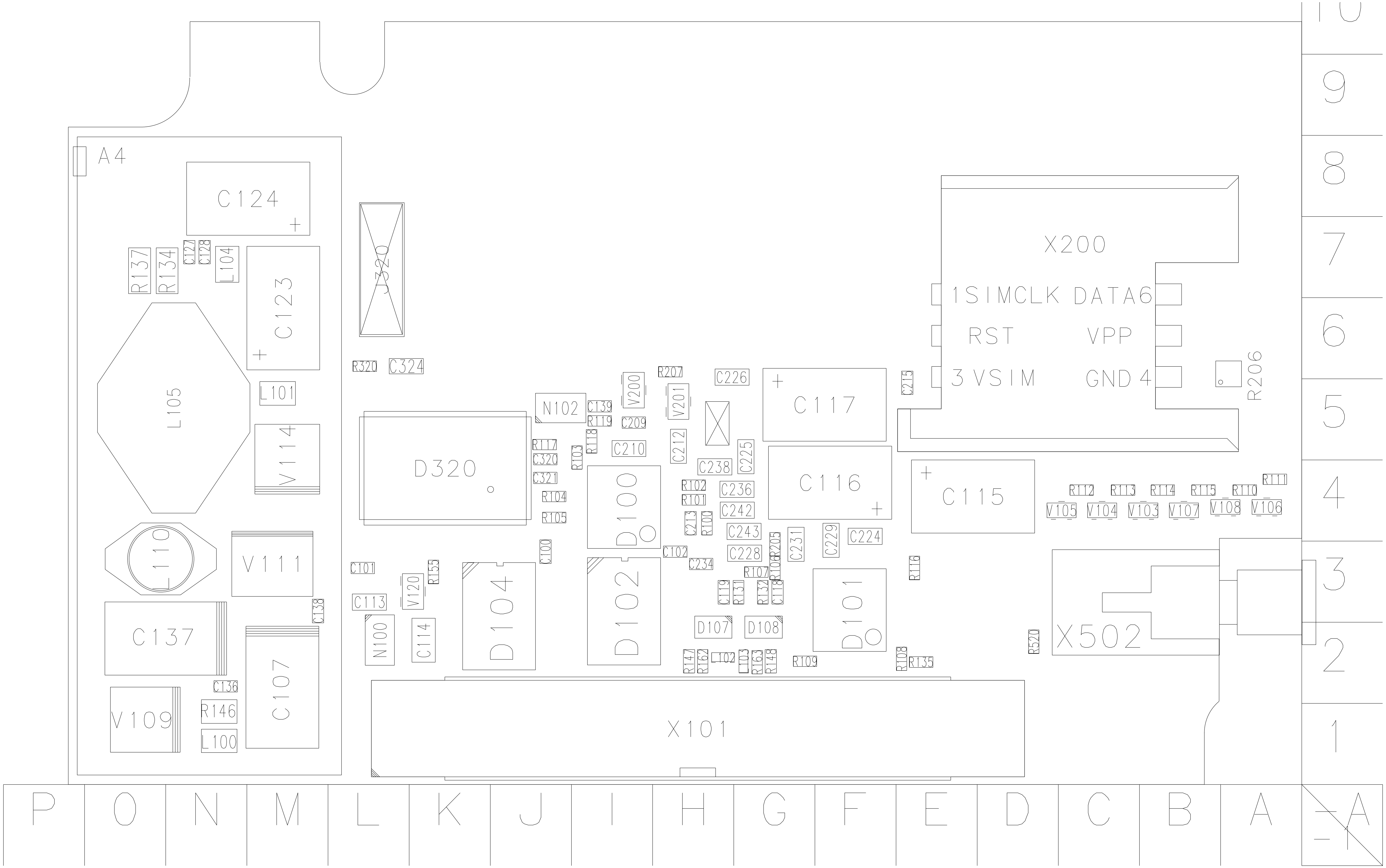
Diagram of RF ground points, V. RB5.0 ed.34


RF GLOBAL GND HOLES
E500 E501 E502 E504 E505 E506 E507 E509 E510 E518 E519
rise
GND
E520 E526 E527 E528 E531 E532 E533 E535 E536 E537 E539
E540 E542 E543 E544 E545 E546 E547 E549 E551 E553 E554 E555 E556 E558
E561 E564 E569 E571 E572 E573 E574 E575 E576 E577 E578
E580 E581 E582 E583 E584 E585 E586 E587 E588 E589 E590 E591 E592 E593 E597 E598
SYSTEM GLOBAL GND HOLES
E105 E114 E117
A1
RF SHIELD 1A
DMC04003
RAULI
A4
RF SHIELD 3
DMC04001
RAULI
A3
RF SHIELD 4
DMC04002
RAULI
A5
RF SHIELD 2
DMC04000
RAULI

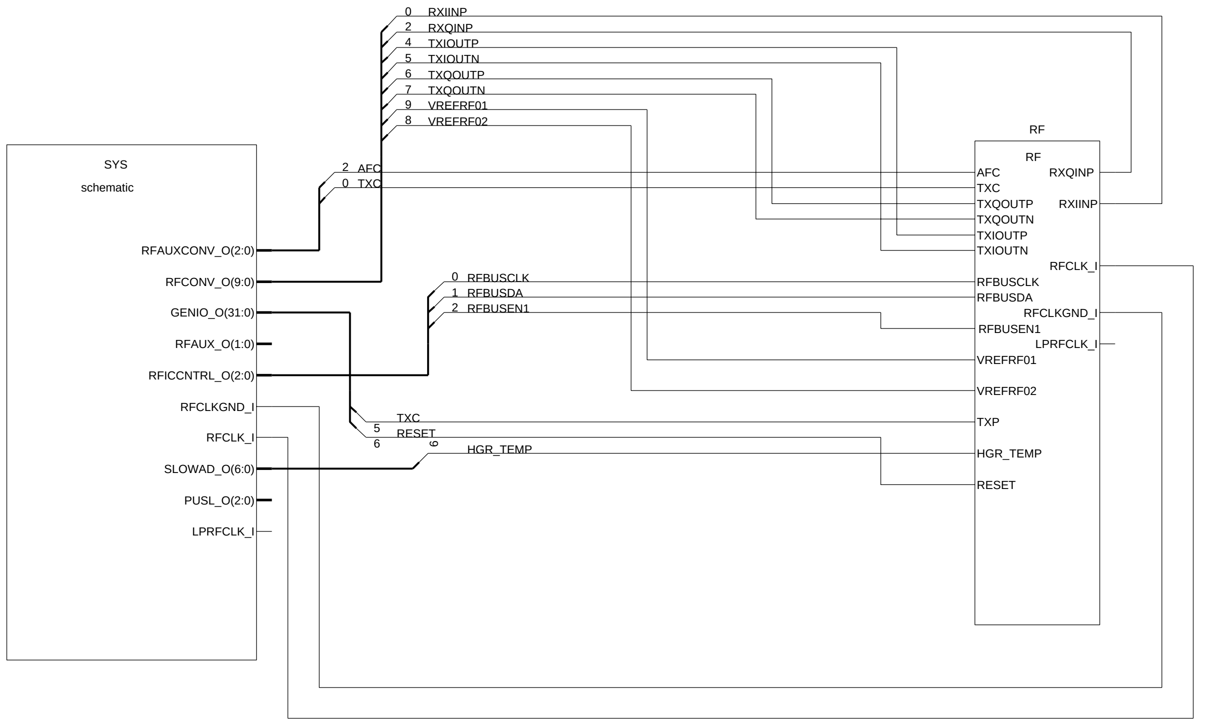
Parts Placement 1/2 RL7_11


10
9
8
7
6
5
4
3
2
1
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
A1
A3
A5
Z500
Z520
V500
V550
V750
L750
N700
L708
L703
C709
V100
V101
V102
L704
R705
Z501
Z551
T700
Z700
N600
R600
G660
G650
T650
C752
R701
R608
D200
D300
B200
J300
Z101
Z100
D103
D105
D106
V115
X501
L109
L108
V112
F101
V118
F100
L107
L106
X100
C131
V110
N101
R144
R145
R150
C126
C120
R164
C121
C134
C133
C104
C103
R149
C111
R125
C112
R129
R143
C130
R141
R142
C129
C135
C220
L202
C201
L203
L200
C222
C208
C203
C219
L201
C200
C202
C204
C322
C303
C302
C239
C241
C240
C237
C216
C244
C230
C227
C246
L204
C214
C109
C110
C235
C232
R153
C233
R161
R154
C300
R204
R202
C207
R160
R157
R158
R151
C305
R401
R400
C401
C400
C221
C223
C217
C105
C323
C218
C247
L205
R159
R156
C211
C206
C205
C301

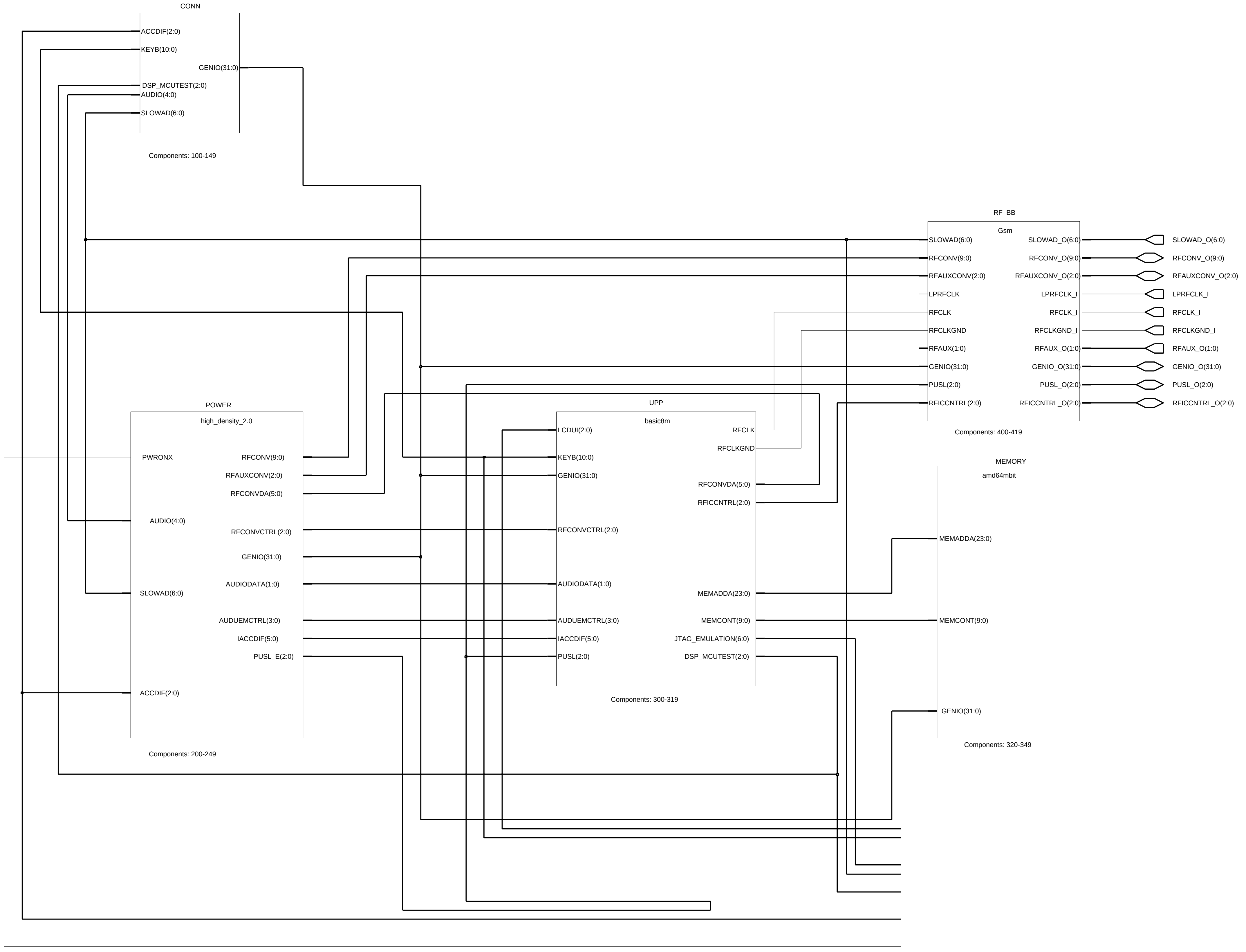
Parts Placement 2/2 RL7_11


A4
C124
R137
R134
C127
C128
L104
C123
J320
L105
L101
V114
R320
C324
N102
C139
R119
V200
R207
V201
C209
C226
C117
C215
X200
1SIMCLK DATA6
RST VPP
3VSIM GND4
R206
D320
R117
C320
C321
R104
R105
R103
R118
C210
C212
C238
C225
C116
C115
R102
R101
C236
C242
C243
C228
C213
R100
R205
R106
C231
C229
C224
R112
R113
R114
R115
R110
R111
V105
V104
V103
V107
V108
V106
D100
C102
C234
R107
R116
X502
L110
V111
C101
C138
C113
V120
R155
C100
D104
D102
C119
R131
R132
C118
D101
C137
N100
C114
D107
D108
R520
C107
C136
V109
R146
L100
R147
R162
L102
L103
R163
R148
R109
R108
R135
X101
P O N M L K J I H G F E D C B A
10 9 8 7 6 5 4 3 2 1
A
1

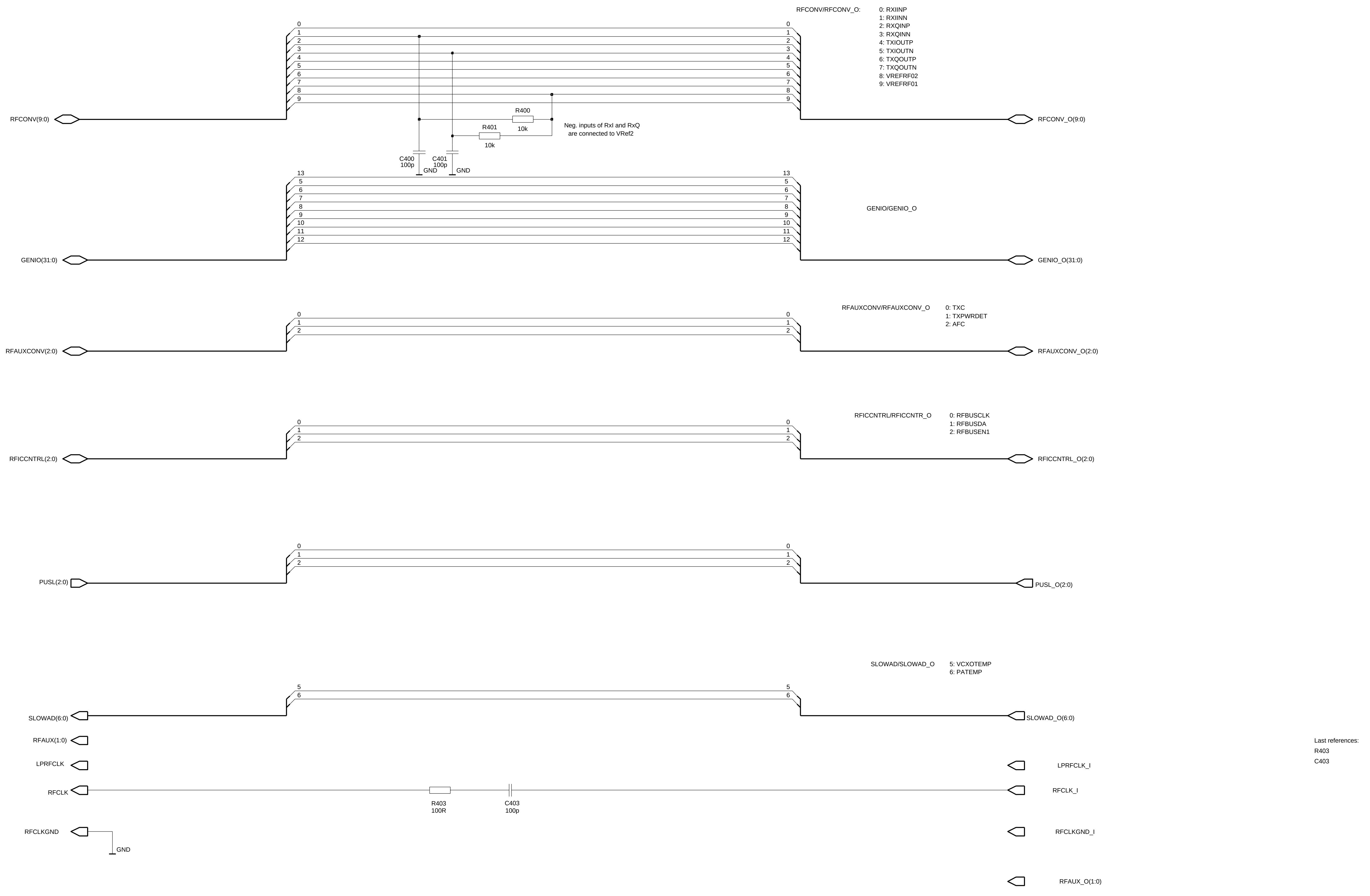
Block diagram v.RB6.0 ed.79


0 RXIINP
2 RXQINP
4 TXIOUTP
5 TXIOUTN
6 TXQOUTP
7 TXQOUTN
9 VREFRF01
8 VREFRF02
RF
SYS
schematic
2 AFC
0 TXC
RF
AFC
TXC
TXQOUTP
TXQOUTN
TXIOUTP
TXIOUTN
RXQINP
RXIINP
RFAUXCONV_O(2:0)
RFCONV_O(9:0)
GENIO_O(31:0)
RFAUX_O(1:0)
RFICCNTRL_O(2:0)
RFCLKGND_I
RFCLK_I
SLOWAD_O(6:0)
PUSL_O(2:0)
LPRFCLK_I
0 RFBUSCLK
1 RFBUSDA
2 RFBUSEN1
RFCLK_I
RFBUSCLK
RFBUSDA
RFCLKGND_I
RFBUSEN1
LPRFCLK_I
VREFRF01
VREFRF02
TXC
5 RESET
6
6
HGR_TEMP
TXP
HGR_TEMP
RESET

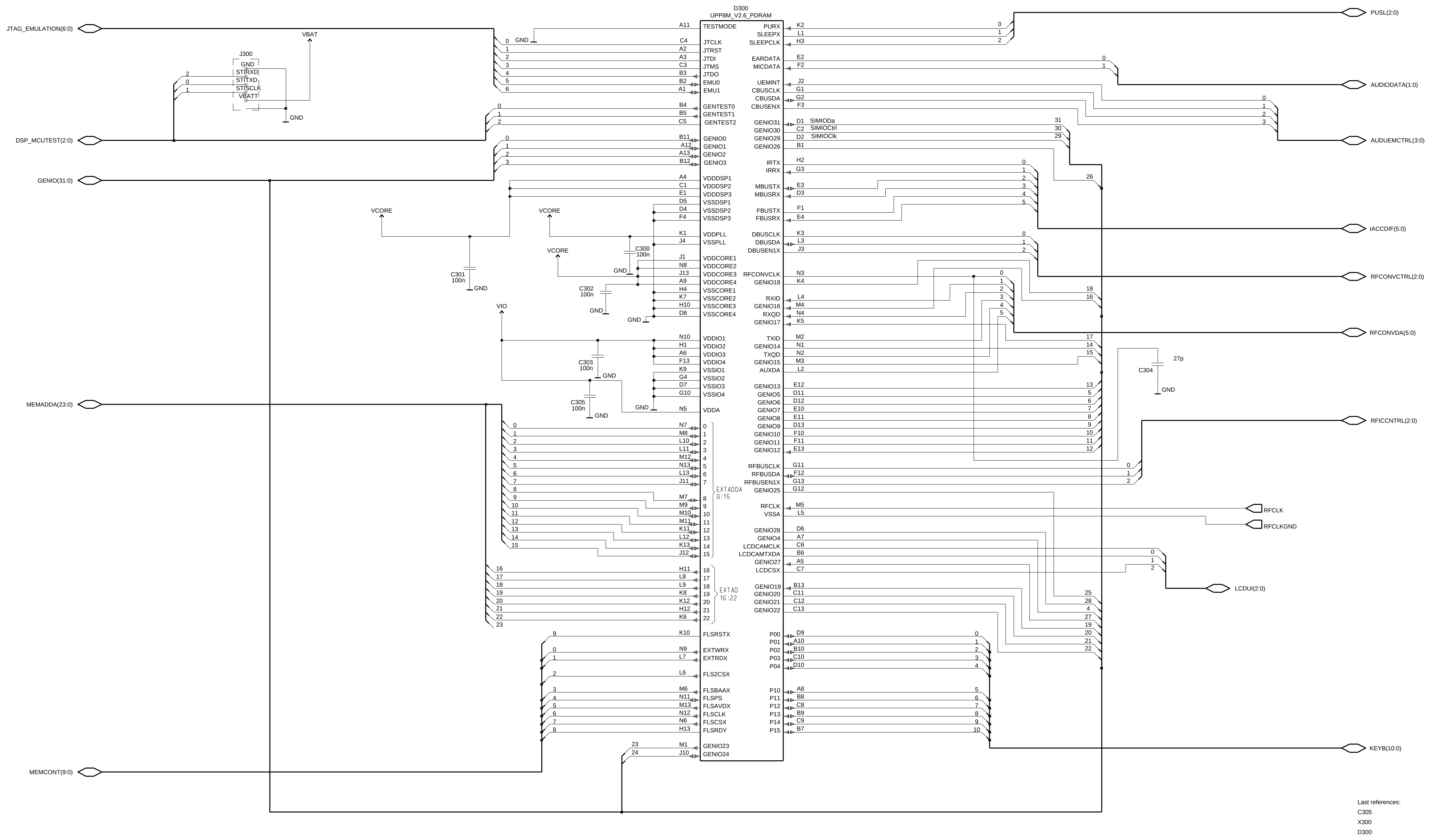
Block Diagram System v.RB6.0 ed.131


CONN
ACCDIF(2:0)
KEYB(10:0)
GENIO(31:0)
DSP_MCUTEST(2:0)
AUDIO(4:0)
SLOWAD(6:0)
Components: 100-149
RF_BB
Gsm
SLOWAD(6:0)
RFCONV(9:0)
RFAUXCONV(2:0)
LPRFCLK
RFCLK
RFCLKGND
RFAUX(1:0)
GENIO(31:0)
PUSL(2:0)
RFICCNTRL(2:0)
SLOWAD_O(6:0)
RFCONV_O(9:0)
RFAUXCONV_O(2:0)
LPRFCLK_I
RFCLK_I
RFCLKGND_I
RFAUX_O(1:0)
GENIO_O(31:0)
PUSL_O(2:0)
RFICCNTRL_O(2:0)
SLOWAD_O(6:0)
RFCONV_O(9:0)
RFAUXCONV_O(2:0)
LPRFCLK_I
RFCLK_I
RFCLKGND_I
RFAUX_O(1:0)
GENIO_O(31:0)
PUSL_O(2:0)
RFICCNTRL_O(2:0)
Components: 400-419
POWER
high_density_2.0
PWRONX
RFCONV(9:0)
RFAUXCONV(2:0)
RFCONVDA(5:0)
AUDIO(4:0)
RFCONVCTRL(2:0)
GENIO(31:0)
AUDIODATA(1:0)
SLOWAD(6:0)
AUDUEMCTRL(3:0)
IACCDIF(5:0)
PUSL_E(2:0)
ACCDIF(2:0)
Components: 200-249
UPP
basic8m
LCDUI(2:0)
RFCLK
RFCLKGND
KEYB(10:0)
GENIO(31:0)
RFCONVDA(5:0)
RFICCNTRL(2:0)
RFCONVCTRL(2:0)
AUDIODATA(1:0)
MEMADDA(23:0)
AUDUEMCTRL(3:0)
MEMCONT(9:0)
IACCDIF(5:0)
JTAG_EMULATION(6:0)
PUSL(2:0)
DSP_MCUTEST(2:0)
Components: 300-319
MEMORY
amd64mbit
MEMADDA(23:0)
MEMCONT(9:0)
GENIO(31:0)
Components: 320-349

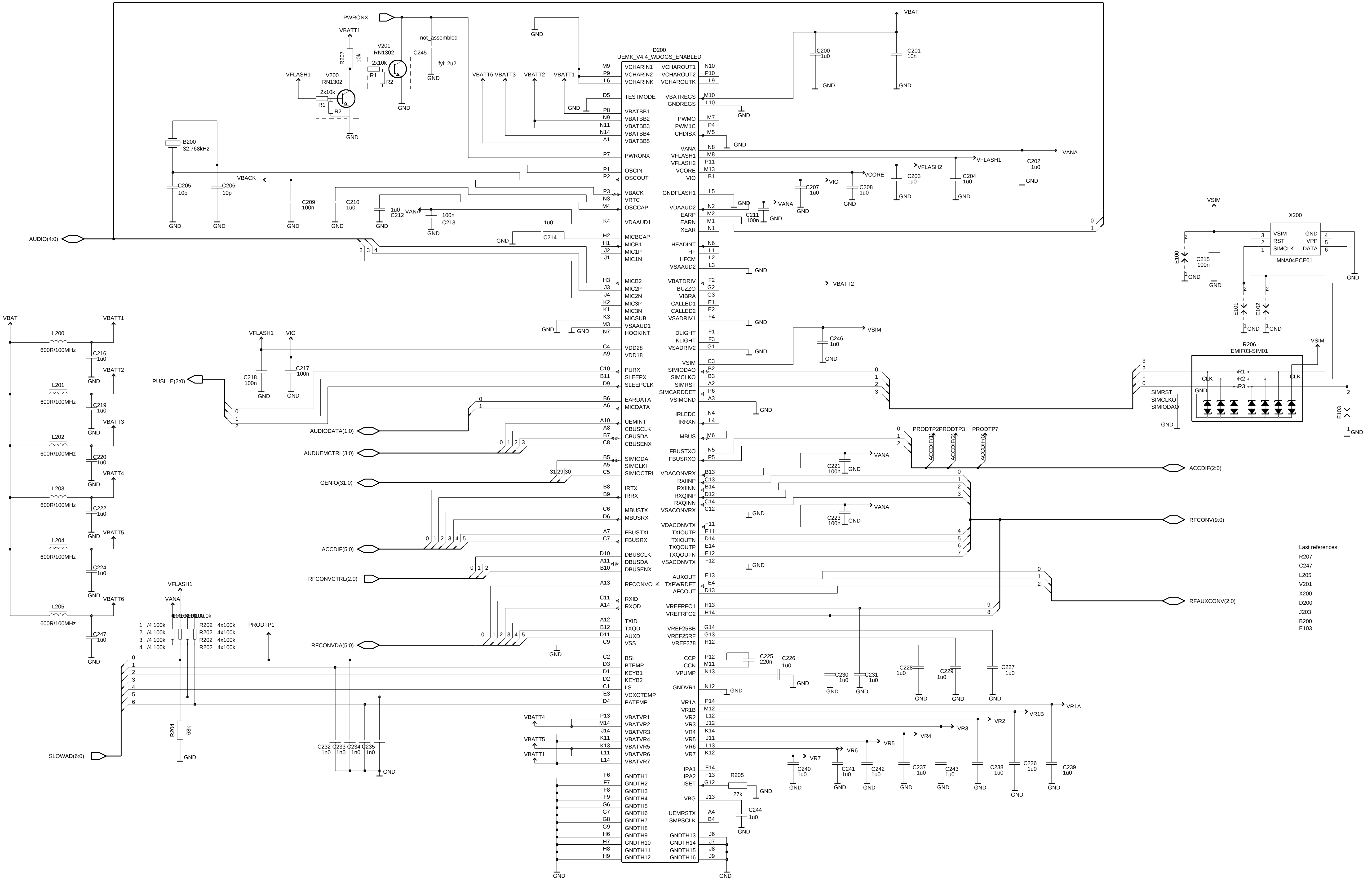
Schematic diagram RF-BB v.RB6.0 ed.22


RFCONV/RFCONV_O:
0: RXIINP
1: RXIINN
2: RXQINP
3: RXQINN
4: TXIOUTP
5: TXIOUTN
6: TXQOUTP
7: TXQOUTN
8: VREFRF02
9: VREFRF01
0
1
2
3
4
5
6
7
8
9
RFCONV(9:0)
RFCONV_O(9:0)
R400
10k
R401
10k
Neg. inputs of RxI and RxQ
are connected to VRef2
C400
100p
C401
100p
GND
GND
13
5
6
7
8
9
10
11
12
GENIO/GENIO_O
GENIO(31:0)
GENIO_O(31:0)
RFAUXCONV/RFAUXCONV_O
0: TXC
1: TXPWRDET
2: AFC
RFAUXCONV(2:0)
RFAUXCONV_O(2:0)
RFICCNTRL/RFICCNTR_O
0: RFBUSCLK
1: RFBUSDA
2: RFBUSEN1
RFICCNTRL(2:0)
RFICCNTRL_O(2:0)
PUSL(2:0)
PUSL_O(2:0)
SLOWAD/SLOWAD_O
5: VCXOTEMP
6: PATEMP
SLOWAD(6:0)
SLOWAD_O(6:0)
RFAUX(1:0)
LPRFCLK
LPRFCLK_I
RFCLK
RFCLK_I
R403
100R
C403
100p
RFCLKGND
RFCLKGND_I
GND
RFAUX_O(1:0)
Last references:
R403
C403

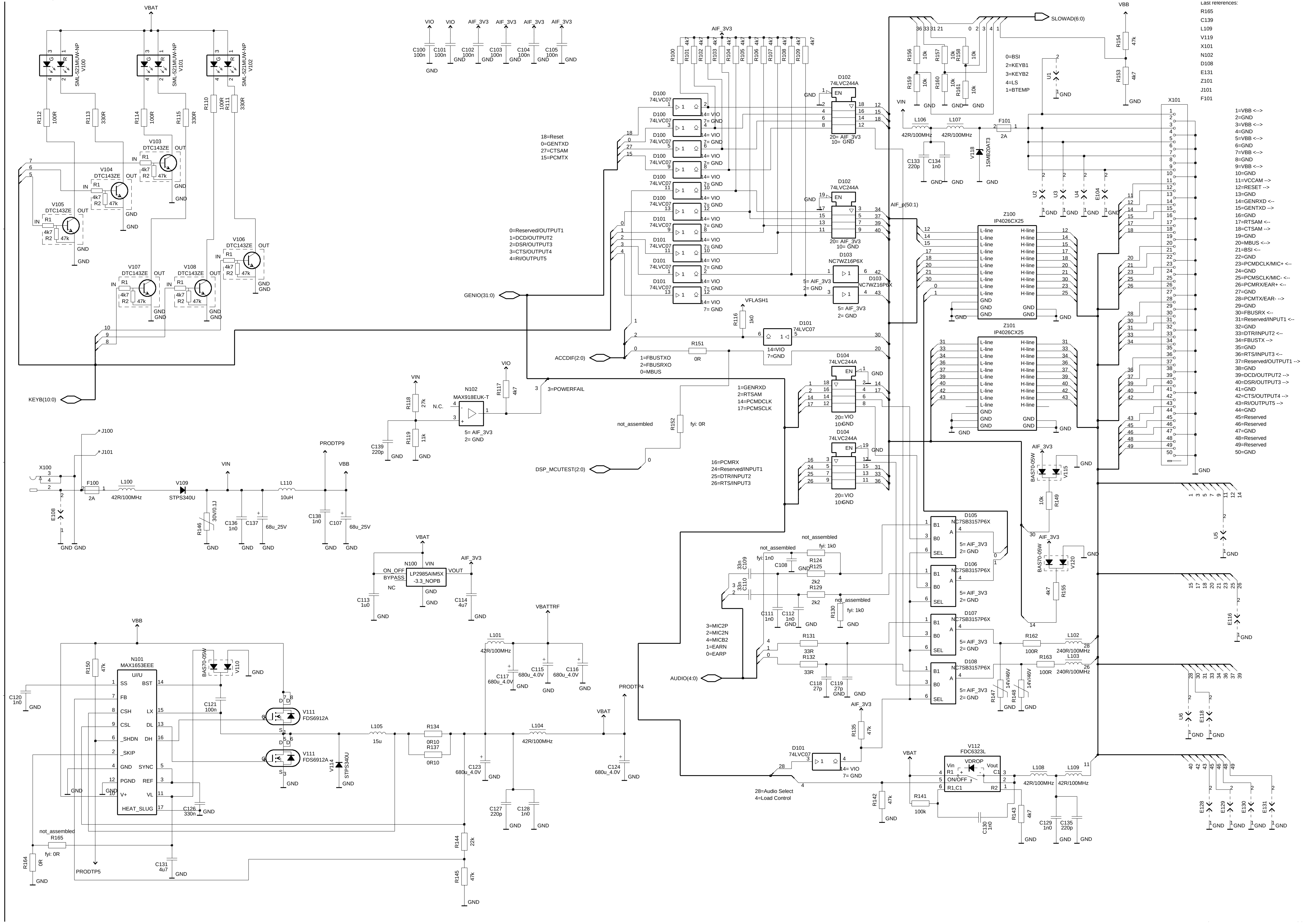
Schematic Diagram UPP v.RB6.0 ed.29


D300
UPP8M_V2.6_PDRAM
JTAG_EMULATION(6:0)
DSP_MCUTEST(2:0)
GENIO(31:0)
MEMADDA(23:0)
MEMCONT(9:0)
PUSL(2:0)
AUDIODATA(1:0)
AUDUEMCTRL(3:0)
IACCDIF(5:0)
RFCONVCTRL(2:0)
RFCONVDA(5:0)
RFICCNTRL(2:0)
RFCLK
RFCLKGND
LCDUI(2:0)
KEYB(10:0)
J300
GND
STIRXD
STITXD
STISCLK
VBATT
VBAT
VCORE
VIO
C300
C301
C302
C303
C304
C305
100n
27p
TESTMODE
JTCLK
JTRST
JTDI
JTMS
JTDO
EMU0
EMU1
GENTEST0
GENTEST1
GENTEST2
GENIO0
GENIO1
GENIO2
GENIO3
VDDDSP1
VDDDSP2
VDDDSP3
VSSDSP1
VSSDSP2
VSSDSP3
VDDPLL
VSSPLL
VDDCORE1
VDDCORE2
VDDCORE3
VDDCORE4
VSSCORE1
VSSCORE2
VSSCORE3
VSSCORE4
VDDIO1
VDDIO2
VDDIO3
VDDIO4
VSSIO1
VSSIO2
VSSIO3
VSSIO4
VDDA
EXTADDA 0:15
EXTAD 16:22
FLSRSTX
EXTWRX
EXTRDX
FLS2CSAX
FLSBAAX
FLSPS
FLSAVDX
FLSCLK
FLSCSX
FLSRDY
GENIO23
GENIO24
PURX
SLEEPX
SLEEPCLK
EARDATA
MICDATA
UEMINT
CBUSCLK
CBUSDA
CBUSENX
GENIO31
GENIO30
GENIO29
GENIO26
SIMIODa
SIMIOCtrl
SIMIOClk
IRTX
IRRX
MBUSTX
MBUSRX
FBUSTX
FBUSRX
DBUSCLK
DBUSDA
DBUSEN1X
RFCONVCLK
GENIO18
RXID
GENIO16
RXQD
GENIO17
TXID
GENIO14
TXQD
GENIO15
AUXDA
GENIO13
GENIO5
GENIO6
GENIO7
GENIO8
GENIO9
GENIO10
GENIO11
GENIO12
RFBUSCLK
RFBUSDA
RFBUSEN1X
GENIO25
RFCLK
VSSA
GENIO28
GENIO4
LCDCAMCLK
LCDCAMTXDA
GENIO27
LCDCSX
GENIO19
GENIO20
GENIO21
GENIO22
P00
P01
P02
P03
P04
P10
P11
P12
P13
P14
P15
Last references:
C305
X300
D300

Schematic Diagram UEM v. RB6.0 ed. 80

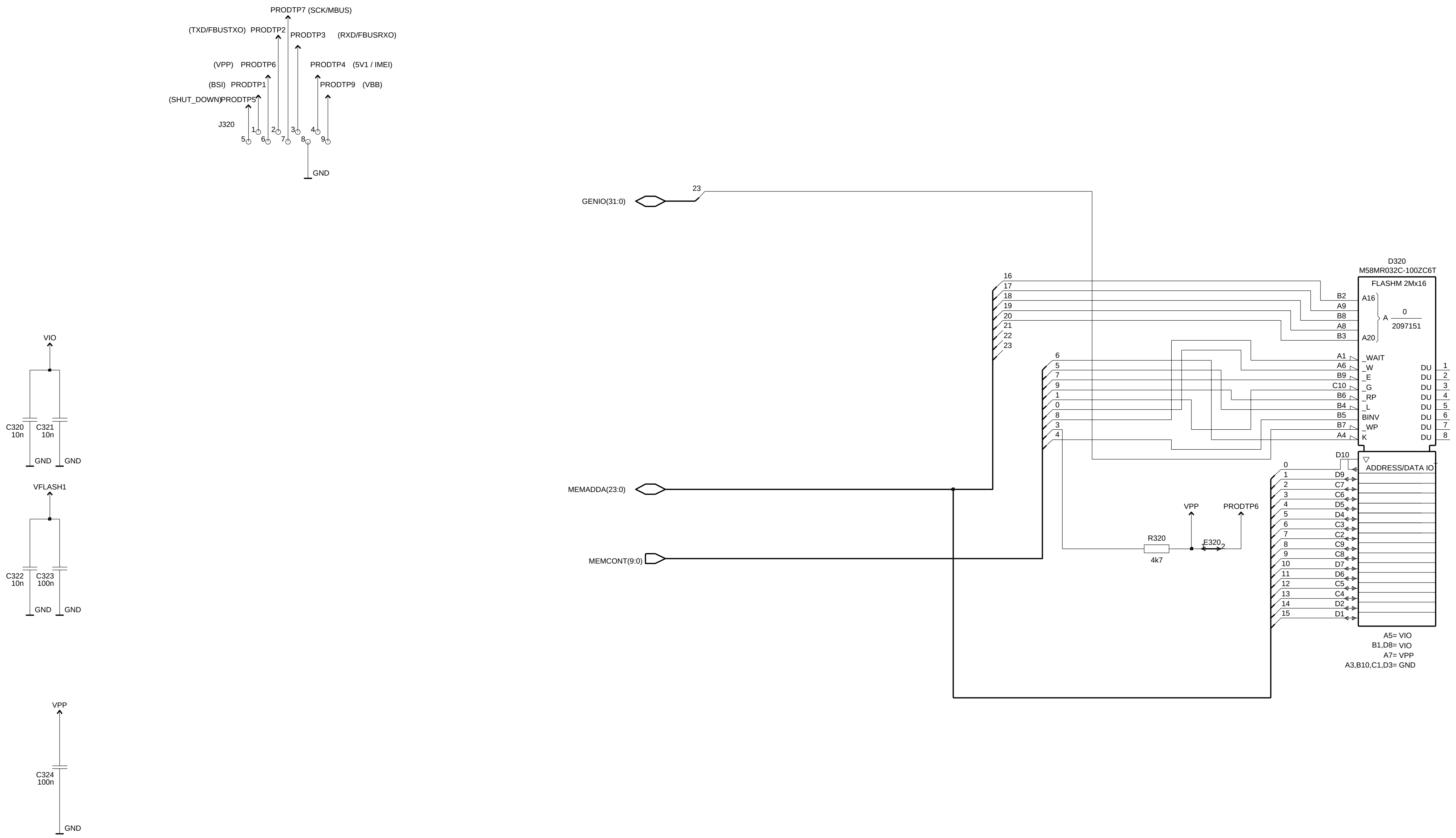

D200
UEMK_V4.4_WDOGS_ENABLED
VCHARIN1
VCHARIN2
VCHARINK
VCHAROUT1
VCHAROUT2
VCHAROUTK
TESTMODE
VBATREGS
GNDREGS
VBATBB1
VBATBB2
VBATBB3
VBATBB4
VBATBB5
PWMO
PWM1C
CHDISX
PWRONX
VANA
VFLASH1
VFLASH2
VCORE
VIO
OSCIN
OSCOUT
VBACK
VRTC
OSCCAP
GNDFLASH1
VDAAUD2
EARP
EARN
XEAR
VDAAUD1
MICBCAP
MICB1
MIC1P
MIC1N
HEADINT
HF
HFCM
VSAAUD2
MICB2
MIC2P
MIC2N
MIC3P
MIC3N
MICSUB
VSAAUD1
HOOKINT
VBATDRIV
BUZZO
VIBRA
CALLED1
CALLED2
VSADRIV1
DLIGHT
KLIGHT
VSADRIV2
VDD28
VDD18
VSIM
PURX
SLEEPX
SLEEPCLK
SIMIODAO
SIMCLKO
SIMRST
SIMCARDDET
VSIMGND
EARDATA
MICDATA
IRLEDC
IRRXN
UEMINT
CBUSCLK
CBUSDA
CBUSENX
MBUS
FBUSTXO
FBUSRXO
SIMIODAI
SIMCLKI
SIMIOCTRL
VDACONVRX
RXIINP
RXIINN
RXQINP
RXQINN
VSACONVRX
IRTX
IRRX
MBUSTX
MBUSRX
VDACONVTX
TXIOUTP
TXIOUTN
TXQOUTP
TXQOUTN
VSACONVTX
FBUSTXI
FBUSRXI
DBUSCLK
DBUSDA
DBUSENX
AUXOUT
TXPWRDET
AFCOUT
RFCONVCLK
RXID
RXQD
VREFRFO1
VREFRFO2
TXID
TXQD
AUXD
VSS
VREF25BB
VREF25RF
VREF278
BSI
BTEMP
KEYB1
KEYB2
LS
VCXOTEMP
PATEMP
CCP
CCN
VPUMP
GNDVR1
VR1A
VR1B
VR2
VR3
VR4
VR5
VR6
VR7
VBATVR1
VBATVR2
VBATVR3
VBATVR4
VBATVR5
VBATVR6
VBATVR7
IPA1
IPA2
ISET
VBG
UEMRSTX
SMPSCLK
GNDTH1
GNDTH2
GNDTH3
GNDTH4
GNDTH5
GNDTH6
GNDTH7
GNDTH8
GNDTH9
GNDTH10
GNDTH11
GNDTH12
GNDTH13
GNDTH14
GNDTH15
GNDTH16
PWRONX
VBATT1
R207
10k
V201
RN1302
2x10k
R1
R2
C245
not_assembled
fyi: 2u2
VFLASH1
V200
RN1302
B200
32.768kHz
C205
10p
C206
10p
VBACK
C209
100n
C210
1u0
C212
1u0
VANA
C213
100n
C214
1u0
AUDIO(4:0)
VBAT
VBATT1
L200
600R/100MHz
C216
1u0
VBATT2
L201
C219
VBATT3
L202
C220
VBATT4
L203
C222
VBATT5
L204
C224
VBATT6
L205
C247
VFLASH1
VIO
C218
100n
C217
100n
PUSL_E(2:0)
AUDIODATA(1:0)
AUDUEMCTRL(3:0)
GENIO(31:0)
IACCDIF(5:0)
RFCONVCTRL(2:0)
RFCONVDA(5:0)
VANA
R202 4x100k
PRODTP1
R204
68k
SLOWAD(6:0)
C232 1n0
C233 1n0
C234 1n0
C235 1n0
VBATT4
VBATT5
VBATT1
VBATT6 VBATT3 VBATT2 VBATT1
C200
1u0
C201
10n
C202
1u0
C203
1u0
C204
1u0
C207
1u0
C208
1u0
C211
100n
VBATT2
C246
1u0
VSIM
C221
100n
C223
100n
PRODTP2
PRODTP3
PRODTP7
ACCDIF(1)
ACCDIF(2)
ACCDIF(0)
ACCDIF(2:0)
RFCONV(9:0)
RFAUXCONV(2:0)
C225
220n
C226
1u0
C228
1u0
C229
1u0
C227
1u0
C230
1u0
C231
1u0
R205
27k
C244
1u0
C240
1u0
C241
1u0
C242
1u0
C237
1u0
C243
1u0
C238
1u0
C236
1u0
C239
1u0
X200
VSIM
RST
SIMCLK
GND
VPP
DATA
MNA04ECE01
C215
100n
E100
E101
E102
E103
R206
EMIF03-SIM01
CLK
SIMRST
SIMCLKO
SIMIODAO
GND
Last references:
R207
C247
L205
V201
X200
D200
J203
B200
E103

Schematic diagram AIF, PWR, LED v. RB6.0 ed.135

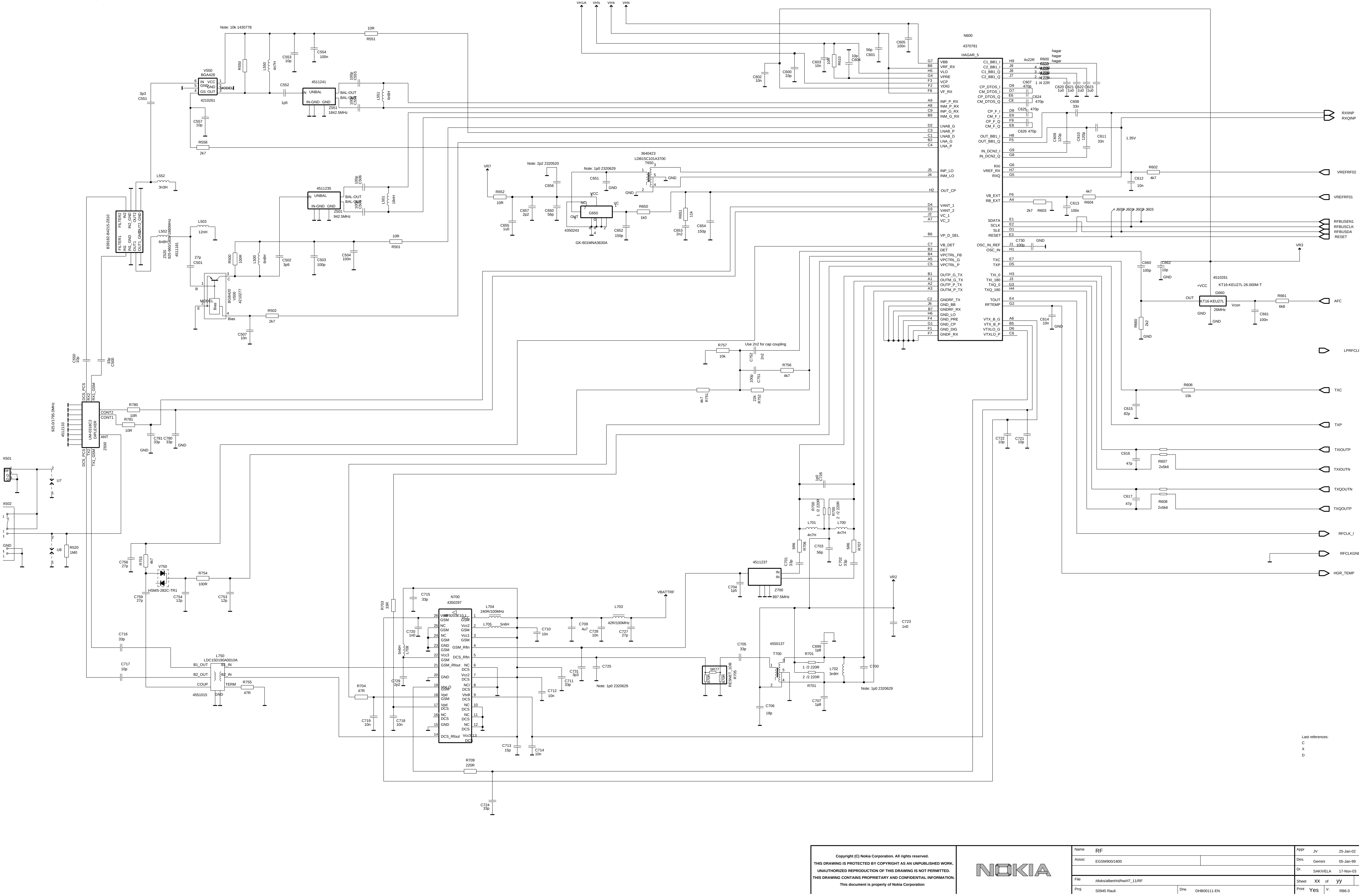

VBAT
SML-521MUW-NP V100
SML-521MUW-NP V101
SML-521MUW-NP V102
R112 100R
R113 330R
R114 100R
R115 330R
R110 100R
R111 330R
V103 DTC143ZE
V104 DTC143ZE
V105 DTC143ZE
V106 DTC143ZE
V107 DTC143ZE
V108 DTC143ZE
KEYB(10:0)
GENIO(31:0)
ACCDIF(2:0)
DSP_MCUTEST(2:0)
AUDIO(4:0)
SLOWAD(6:0)
AIF_p(50:1)
18=Reset
0=GENTXD
27=CTSAM
15=PCMTX
0=Reserved/OUTPUT1
1=DCD/OUTPUT2
2=DSR/OUTPUT3
3=CTS/OUTPUT4
4=RI/OUTPUT5
1=FBUSTXO
2=FBUSRXO
0=MBUS
1=GENRXD
2=RTSAM
14=PCMDCLK
17=PCMSCLK
16=PCMRX
24=Reserved/INPUT1
25=DTR/INPUT2
26=RTS/INPUT3
3=MIC2P
2=MIC2N
4=MICB2
1=EARN
0=EARP
28=Audio Select
4=Load Control
0=BSI
2=KEYB1
3=KEYB2
4=LS
1=BTEMP
3=POWERFAIL
not_assembled
D100 74LVC07
D101 74LVC07
D102 74LVC244A
D103 NC7WZ16P6X
D104 74LVC244A
D105 NC7SB3157P6X
D106 NC7SB3157P6X
D107 NC7SB3157P6X
D108 NC7SB3157P6X
Z100 IP4026CX25
Z101 IP4026CX25
N100 LP2985AIM5X-3.3_NOPB
N101 MAX1653EEE
N102 MAX918EUK-T
V109 STPS340U
V110 BAS70-05W
V111 FDS6912A
V112 FDC6323L
V114 STPS340U
V115 BAS70-05W
V118 1SMB20AT3
V120 BAS70-05W
X100
X101
J100
J101
F100 2A
F101 2A
L100 42R/100MHz
L101 42R/100MHz
L102 240R/100MHz
L103 240R/100MHz
L104 42R/100MHz
L105 15u
L106 42R/100MHz
L107 42R/100MHz
L108 42R/100MHz
L109 42R/100MHz
L110 10uH
VIO
VIN
VBB
VBATTRF
VFLASH1
AIF_3V3
PRODTP4
PRODTP5
PRODTP9
GND
Last references:
R165
C139
L109
V119
X101
N102
D108
E131
Z101
J101
F101
1=VBB <-->
2=GND
3=VBB <-->
4=GND
5=VBB <-->
6=GND
7=VBB <-->
8=GND
9=VBB <-->
10=GND
11=VCCAM -->
12=RESET -->
13=GND
14=GENRXD <--
15=GENTXD -->
16=GND
17=RTSAM <--
18=CTSAM -->
19=GND
20=MBUS <-->
21=BSI <--
22=GND
23=PCMDCLK/MIC+ <--
24=GND
25=PCMSCLK/MIC- <--
26=PCMRX/EAR+ <--
27=GND
28=PCMTX/EAR- -->
29=GND
30=FBUSRX <--
31=Reserved/INPUT1 <--
32=GND
33=DTR/INPUT2 <--
34=FBUSTX -->
35=GND
36=RTS/INPUT3 <--
37=Reserved/OUTPUT1 -->
38=GND
39=DCD/OUTPUT2 -->
40=DSR/OUTPUT3 -->
41=GND
42=CTS/OUTPUT4 -->
43=RI/OUTPUT5 -->
44=GND
45=Reserved
46=Reserved
47=GND
48=Reserved
49=Reserved
50=GND

Schematic Diagram Memories v. RB6.0 ed.32

Last references:
R320
C324
D320
E320
J320


PRODTP7 (SCK/MBUS)
(TXD/FBUSTXO) PRODTP2
PRODTP3 (RXD/FBUSRXO)
(VPP) PRODTP6
PRODTP4 (5V1 / IMEI)
(BSI) PRODTP1
PRODTP9 (VBB)
(SHUT_DOWN)PRODTP5
J320
1 2 3 4
5 6 7 8 9
GND
VIO
C320 10n
C321 10n
GND GND
VFLASH1
C322 10n
C323 100n
GND GND
VPP
C324 100n
GND
GENIO(31:0)
23
MEMADDA(23:0)
MEMCONT(9:0)
16 17 18 19 20 21 22 23
6 5 7 9 1 0 8 3 4
D320
M58MR032C-100ZC6T
FLASHM 2Mx16
B2 A9 B8 A8 B3
A16 A20
A 0 2097151
A1 A6 B9 C10 B6 B4 B5 B7 A4
_WAIT _W _E _G _RP _L BINV _WP K
DU 1 DU 2 DU 3 DU 4 DU 5 DU 6 DU 7 DU 8
D10
ADDRESS/DATA IO
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
D9 C7 C6 D5 D4 C3 C2 C9 C8 D7 D6 C5 C4 D2 D1
VPP
PRODTP6
R320
4k7
E320
1 2
A5= VIO
B1,D8= VIO
A7= VPP
A3,B10,C1,D3= GND

Schematic Diagram RF, v. RB6.0 ed. 168


N600
4370781
HAGAR_5
V550
BGA428
4210261
4511241
Z551
1842.5MHz
4511235
Z501
942.5MHz
V500
BGR420
4210277
Z550
925-960/1805-1880MHz
4511181
Z500
UM-0318C2
DIPLEXER
925.0/1795.0MHz
4512133
G650
4350243
GK-601MNA3630A
T650
3640423
LDB15C101A3700
G660
4510261
KT16-KEU27L-26.000M-T
26MHz
N700
4350297
4511237
Z700
897.5MHz
T700
4550137
L750
LDC15D190A0010A
4551015
V750
HSMS-282C-TR1
X501
X502
U7
U8
RXIINP
RXQINP
VREFRF02
VREFRF01
RFBUSEN1
RFBUSCLK
RFBUSDA
RESET
AFC
LPRFCLI
TXC
TXP
TXIOUTP
TXIOUTN
TXQOUTN
TXQOUTP
RFCLK_I
RFCLKGNI
HGR_TEMP
VBATTRF
VR2
VR3
VR7
VH1A
VH3
VH4
VH5
Use 2n2 for cap coupling
Note: 10k 1430778
Note: 2p2 2320520
Note: 1p0 2320629
Last references:
C
X
D

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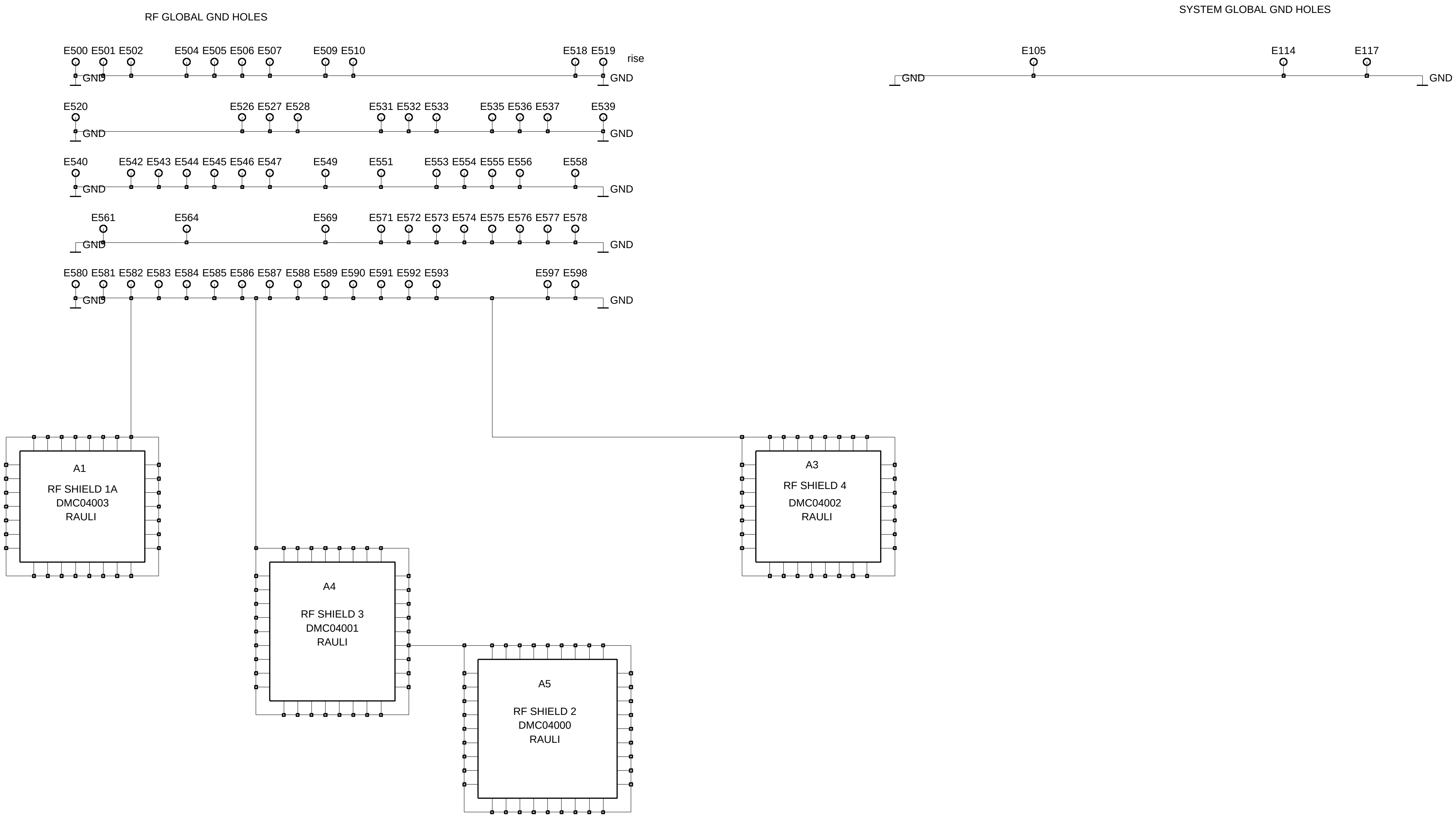
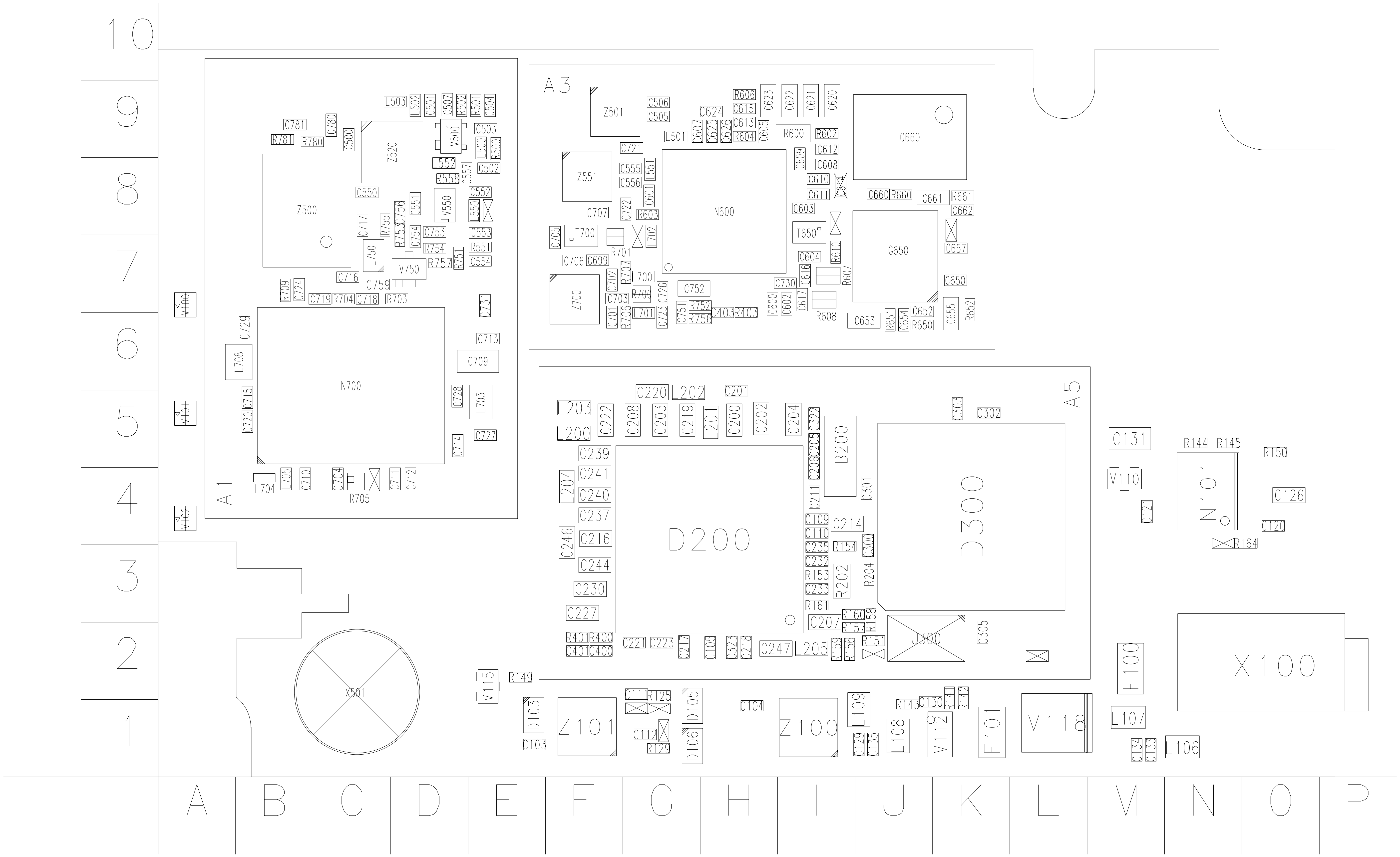
Name	RF	Appr	JV 25-Jan-02
Assoc	EGSM900/1800	Des.	Gemini 05-Jan-99
		Dr.	SAKIVELA 17-Nov-03
File	/disks/albert/rd/hw/rl7_11/RF	Sheet	xx of yy
Proj	S0945 Rauli	Drw. DHB00111-EN	Print Yes V. RB6.0

Diagram of RF ground points, V. RB6.0 ed.41


RF GLOBAL GND HOLES
E500 E501 E502 E504 E505 E506 E507 E509 E510 E518 E519
rise
GND
GND
E520 E526 E527 E528 E531 E532 E533 E535 E536 E537 E539
GND
GND
E540 E542 E543 E544 E545 E546 E547 E549 E551 E553 E554 E555 E556 E558
GND
GND
E561 E564 E569 E571 E572 E573 E574 E575 E576 E577 E578
GND
GND
E580 E581 E582 E583 E584 E585 E586 E587 E588 E589 E590 E591 E592 E593 E597 E598
GND
GND
SYSTEM GLOBAL GND HOLES
E105 E114 E117
GND
GND
A1
RF SHIELD 1A
DMC04003
RAULI
A3
RF SHIELD 4
DMC04002
RAULI
A4
RF SHIELD 3
DMC04001
RAULI
A5
RF SHIELD 2
DMC04000
RAULI

Parts placement diagram, RL7_11a top


10
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5
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2
1
A
B
C
D
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F
G
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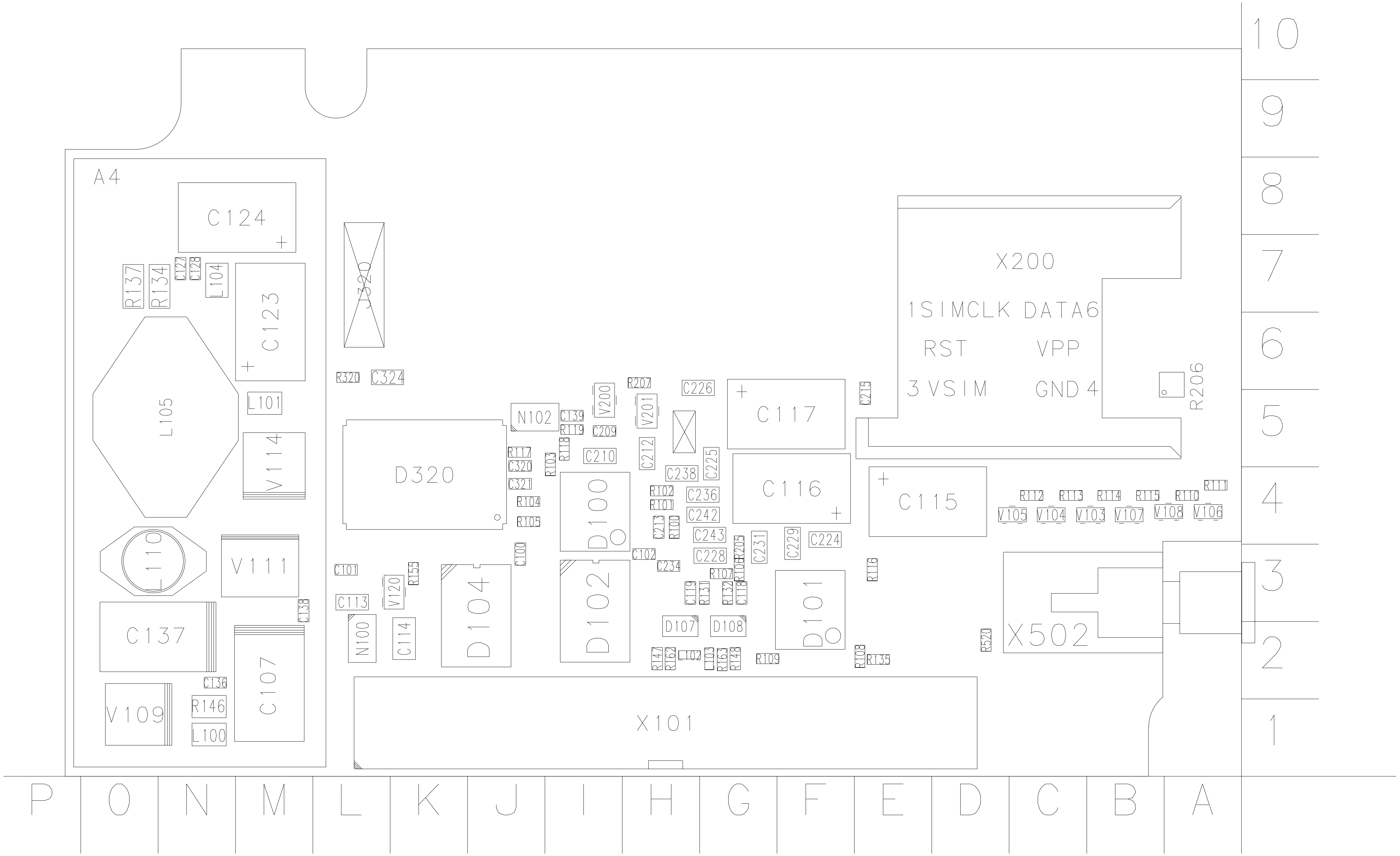
I
J
K
L
M
N
O
P
A1
A3
A5
Z500
Z520
V500
V550
V750
L750
N700
L708
L703
C709
C713
C727
C728
C714
C729
C715
C720
L704
L705
C710
C704
R705
C711
C712
C781
R781
R780
C780
C500
L503
L502
C501
C507
R502
R501
C504
C503
L500
R500
L552
R558
C557
C502
C550
C551
C552
L550
C717
R755
R753
C756
C754
C753
R754
R757
R751
C553
R551
C554
C716
C759
R709
C724
C719
R704
C718
R703
C731
V100
V101
V102
Z501
C506
C505
R606
C615
C613
R604
C623
C622
C621
C620
C624
C607
C625
C626
C605
L501
R600
R602
C612
C608
C609
C610
C611
C614
G660
C721
Z551
C555
C556
L551
C601
C722
R603
C707
C705
T700
R701
C706
C699
C702
R707
C702
L700
R700
Z700
C703
C701
R706
L701
C726
C723
C752
C751
R752
R756
C403
R403
N600
C603
T650
C604
R610
R607
C616
C730
C600
C602
C617
R608
C653
R651
C654
C652
R650
C655
R652
C650
C657
G650
C660
R660
C661
R661
C662
C220
L202
C201
L203
L200
C222
C208
C203
C219
L201
C200
C202
C204
C322
C205
C206
B200
C211
C301
C303
C302
D300
D200
C239
C241
C240
C237
L204
C246
C216
C244
C230
C227
C109
C110
C235
C232
R153
C233
R161
C214
R154
C300
R202
R204
C207
R160
R158
R157
R159
R156
R151
J300
C305
R401
R400
C401
C400
C221
C223
C217
C105
C323
C218
C247
L205
C131
R144
R145
R150
V110
N101
C126
C121
C120
R164
X100
F100
V115
R149
D103
C103
Z101
C111
R125
D105
C112
R129
D106
C104
Z100
L109
C129
C135
L108
R143
C130
R141
R142
V112
F101
V118
L107
C134
C133
L106
X501

Parts Placement bottom RL7_11a Bottom


10
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7
6
5
4
3
2
1
A4
C124
R137
R134
C127
C128
L104
C123
J320
X200
1SIMCLK DATA6
RST VPP
3VSIM GND4
R206
L105
R320
C324
L101
N102
C139
R119
V200
R207
V201
C226
C117
C215
V114
D320
R117
C320
C321
R104
R105
R103
R118
C209
C210
C212
C238
C225
C116
C115
R102
R101
C236
C242
C213
R100
D100
C243
C228
C102
C234
R205
C231
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C224
R112
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R110
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C113
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C114
D107
D108
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R108
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